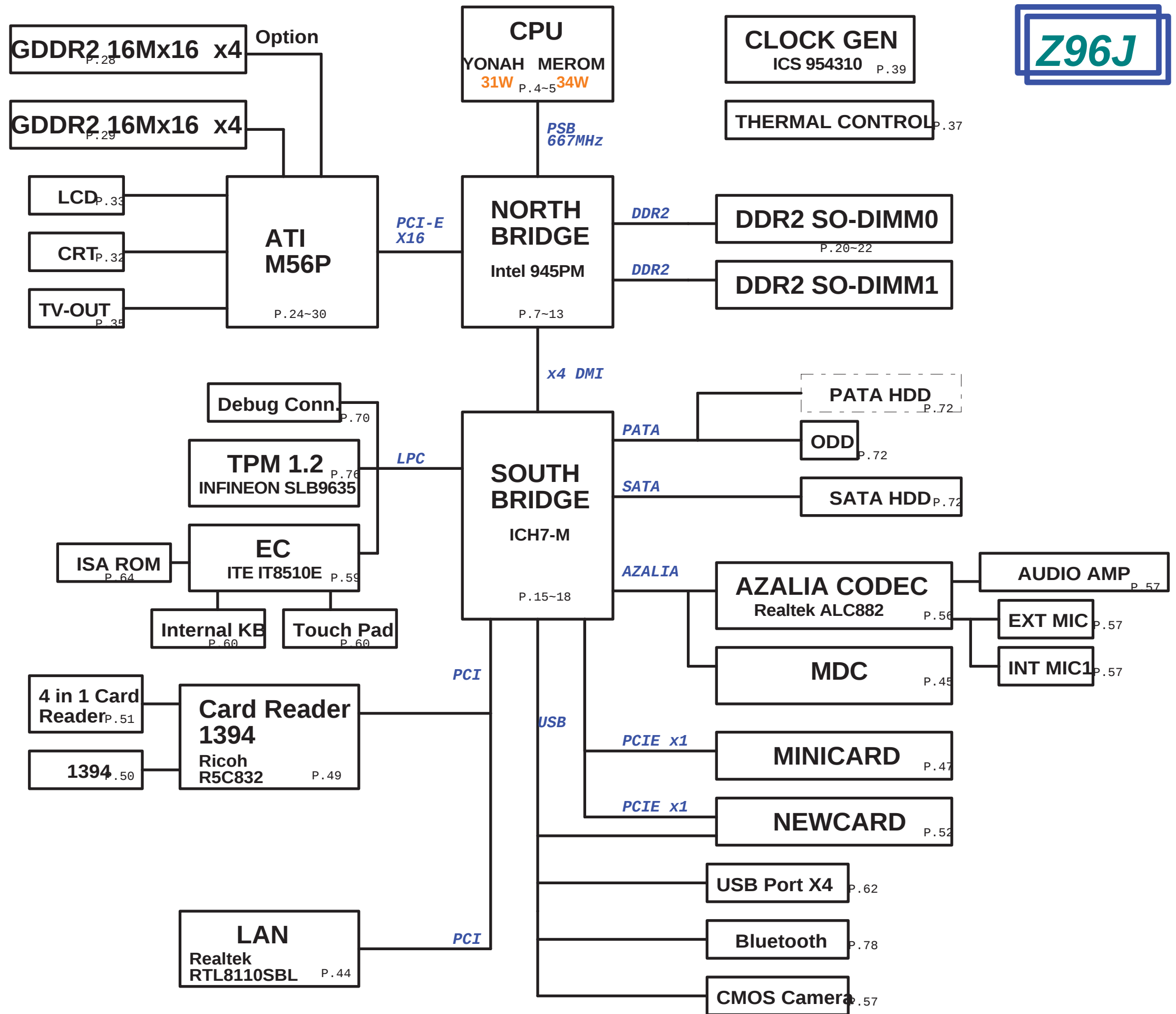




Z96J

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type	Z96J Default	EC Default
32	PWM0/GPA0	/			GPI
33	PWM1/GPA1	FAN_PWM	O	H	GPI
36	PWM2/GPA2	CLK_PWRSAVE#	O		GPI
37	PWM3/GPA3	/			GPI
38	PWM4/GPA4	CHG_LED_UP#	O	H	GPI
39	PWM5/GPA5	PWR_LED_UP#	O	H	GPI
40	PWM6/GPA6	/	O		GPI
43	PWM7/GPA7	LCD_BACKOFF#	O	H	GPI
153	RXD/GPB0	NUM_LED	O	L	GPI
154	TXD/GPB1	CAP_LED	O	L	GPI
162	GPB2	SCRL_LED	O	L	GPI
163	SMCLK0/GPB3	SMB0_CLK	SMCLK0		GPI
164	SMDAT0/GPB4	SMB0_DAT	SMDAT0		GPI
5	GA20/GPB5	A20GATE	GA20		GPO
6	KBRST#/GPB6	RC_IN#	KBRST#		KBRST#
165	GPB7	/	I		GPI
47	CLKOUT/GPC0	/	O		GPI
169	SMCLK1/GPC1	SMB1_CLK	SMCLK1		GPI
170	SMDAT1/GPC2	SMB1_DAT	SMDAT1		GPI
171	GPC3	MAIL_LED	O	L	GPI
172	TMRI0/WUI2/GPC4	/	I		GPI
175	GPC5	OP_SD#	O	H	GPI
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I	H	GPI
1	CK32KOUT/GPC7	/			GPI
26	RI1#/WUI0/GPD0	SUSB#	I		GPI
29	RI2#/WUI1/GPD1	SUSC#	I		GPI
30	LPCRST#/WUI4/GPD2	PLT_RST#	LPCRST		LPCRST
31	ECSCI#/GPD3	EXT_SCI#	ECSCI#	H	GPI
41	GPD4	RF_ON_SW#	O	H	GPI
42	GINT/GPD5	/			GPI
62	TACH0/GPD6	FAN0_TACH	TACH0		GPI
63	TACH1/GPD7	/			GPI
87	ADC4/GPE0	DISTP_SW#	I		GPI
88	ADC5/GPE1	/			GPI
89	ADC6/GPE2	EMAIL_SW#	I		GPI
90	ADC7/GPE3	EXPLORE_SW#	I		GPI
2	PWRSW/GPE4	PWR_SW#	PWRSW		GPI
44	WUI5/GPE5	/			GPI
24	LPCPD#/WUI6/GPE6	LID_EC#	I		GPI
25	CLKRUN#/WUI7/GPE7	/			GPI
110	PS2CLK0/GPF0	/			GPI
111	PS2DAT0/GPF1	/			GPI
114	PS2CLK1/GPF2	/			GPI
115	PS2DAT1/GPF3	/			GPI
116	PS2CLK2/GPF4	TP_CLK	PS2CLK2		GPI
117	PS2DAT2/GPF5	TP_DAT	PS2DAT2		GPI
118	PS2CLK3/GPF6	/			GPI
119	PS2DAT3/GPF7	INTERNET#	I		GPI
113	FA16/GPG0	FA16	FA16		GPI
112	FA17/GPG1	FA17	FA17		GPI
104	FA18/GPG2	FA18	FA18		GPI
103	FA19/GPG3	/			GPI
3	FA20/GPG4	THRM_CPU#	I	H	GPI
4	FA21/GPG5	/			GPI
27	LPC80HL/GPG6	PMTHERM#	O	H	GPI
28	LPC80LL/GPG7	AC_APR_UC#	I	H	GPI

Pin	Pin Name	Signal Name	Type	Default
48	GPH0	VSUS_ON	O	L GPI
54	GPH1	VSUS_GD#	I	H GPI
55	GPH2	CPUPWR_GD#	I	H GPI
69	GPH3	PM_PWRBTN#	O	H GPI
70	GPH4	SUSC_ON	O	L GPI
75	GPH5	SUSB_ON	O	L GPI
76	GPH6	CPU_VRON	O	L GPI
105	GPH7	PM_RSMRST#	O	L GPI
148	GPI0	ICH7_PWROK	O	L GPI
149	GPI1	/	O	GPI
152	GPI2	MCHOK	I	L GPI
155	GPI3	CHG_EN#	O	H GPI
156	GPI4	PRECHG	O	L GPI
168	GPI5	BAT_LL#	O	H GPI
174	GPI6	BAT_LEARN	O	L GPI
93	ADC8	KID0	I	
94	ADC9	KID1	I	
101	DAC2	BL_PWM_DA	O	
102	DAC3	BATSEL_2P#	O	

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	0100110X (98)

PCI Device	IDSEL#	REQ / GNT#	Interrupts
CARD READER	AD17	0	B
1394	AD17	0	A
LAN	AD23	2	C

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type	Power Well	Default
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I	Core(To:3.3V)	GPI
C8	GPIO01/REQ5#	PCI_REQ#5	I/O	Core(To:5V)	GPI
G8	GPIO02/PIRQE#	PCI_INTE#	I(OD)	Core(To:5V)	GPI
F7	GPIO03/PIRQF#	PCI_INTF#	I(OD)	Core(To:5V)	GPI
F8	GPIO04/PIRQG#	PCI_INTG#	I(OD)	Core(To:5V)	GPI
G7	GPIO05/PIRQH#	PCI_INTH#	I(OD)	Core(To:5V)	GPI
AC21	GPIO06	NC	I/O	Core(To:3.3V)	GPI
AC18	GPIO07	WLAN_BT_LED_EN#	O	Core(To:3.3V)	GPI
E21	GPIO08	EXTSMI#	I	SUS(To:3.3V)	GPI
E20	GPIO09	SATA_DET#0	I/O	SUS(To:3.3V)	GPI
A20	GPIO10	WLAN_ON#	O	SUS(To:3.3V)	GPI
B23	SMBALERT#/GPIO11	SMB_ALERT#	I/O	SUS(To:3.3V)	Native
F19	GPIO12	KBC_SCI#	I	SUS(To:3.3V)	GPI
E19	GPIO13	TP	I/O	SUS(To:3.3V)	GPI
R4	GPIO14	NC	I/O	SUS(To:3.3V)	GPI
E22	GPIO15	CB_SD#	I/O	SUS(To:3.3V)	GPI
AC22	GPIO16/DPRSPLPVR	PM_DPRSPLPVR	O	Core(To:3.3V)	Native
D8	GPIO17/GNT5#	PCI_GNT#5	I/O	Core(To:3.3V)	GPO
AC20	GPIO18/STP_PCI#	STP_PCI#	O	Core(To:3.3V)	GPO
AH18	GPIO19/SATA1GP	NC	O	Core(To:3.3V)	GPI
AF21	GPIO20/STP_CPU#	STP_CPU#	O	Core(To:3.3V)	GPO
AE19	GPIO21/SATA0GP	NC	I/O	Core(To:3.3V)	GPI
A13	GPIO22/REQ4#	PCI_REQ#4	I/O	Core(To:3.3V)	Native
AA5	LDRQ1#/GPIO23	TP	I/O	Core(To:3.3V)	Native
R3	GPIO24	NC	I/O	SUS(To:3.3V)	GPO
D20	GPIO25	NC	I/O	SUS(To:3.3V)	GPO
A21	GPIO26/EL_RSVD	NC	I/O	SUS(To:3.3V)	GPO
B21	GPIO27/EL_STATE0	PD_DET#	I/O	SUS(To:3.3V)	GPO
E23	GPIO28/EL_STATE1	NC	I/O	SUS(To:3.3V)	GPO
C3	GPIO29/OC#5	USB_OC#5	I/O	SUS(To:3.3V)	Native
A2	GPIO30/OC#6	NEWCARD_OC#	I	SUS(To:3.3V)	Native
B3	GPIO31/OC#7	USB_OC#7	I/O	SUS(To:3.3V)	Native
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O	Core(To:3.3V)	GPO
AC19	GPIO33/AZ_DOCK_EN#	BT_ON#	O	Core(To:3.3V)	GPO
U2	GPIO34/AZ_DOCK_RST#	NC	I/O	Core(To:3.3V)	GPO
AD21	GPIO35	NC	I/O	Core(To:3.3V)	GPO
AH19	GPIO36/SATA2GP	NC	I/O	Core(To:3.3V)	GPI
AE19	GPIO37/SATA3GP	PCB_ID0	I	Core(To:3.3V)	GPI
AD20	GPIO38	PCB_ID1	I	Core(To:3.3V)	GPI
AE20	GPIO39	PCB_ID2	I	Core(To:3.3V)	GPI
A14	GNT4#/GPIO48	PCI_GNT#4	I/O	Core(To:3.3V)	Native
AG24	GPIO49/CPUPWRGD	H_PWRGD	O	V_CPU_IO	Native

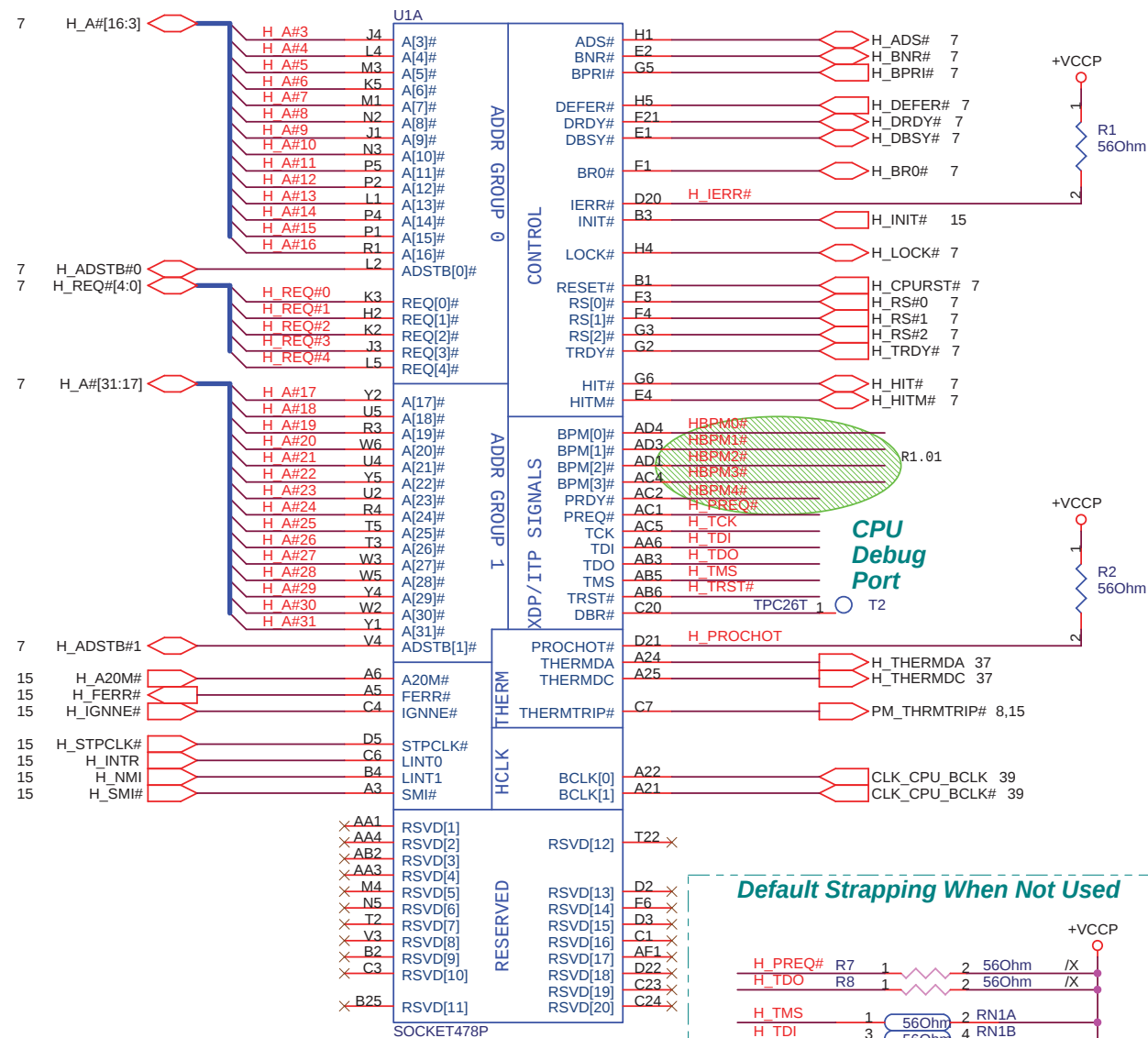


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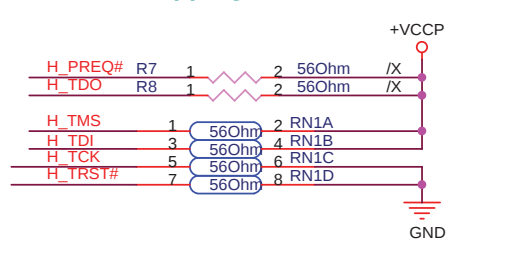
ASUSTek Computer INC. Engineer: Alan Chu

Size	Project Name	Rev
Custom	Z96J	1.0

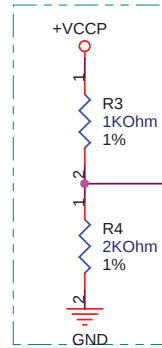
Date: Wednesday, January 11, 2006Sheet 2 of 92



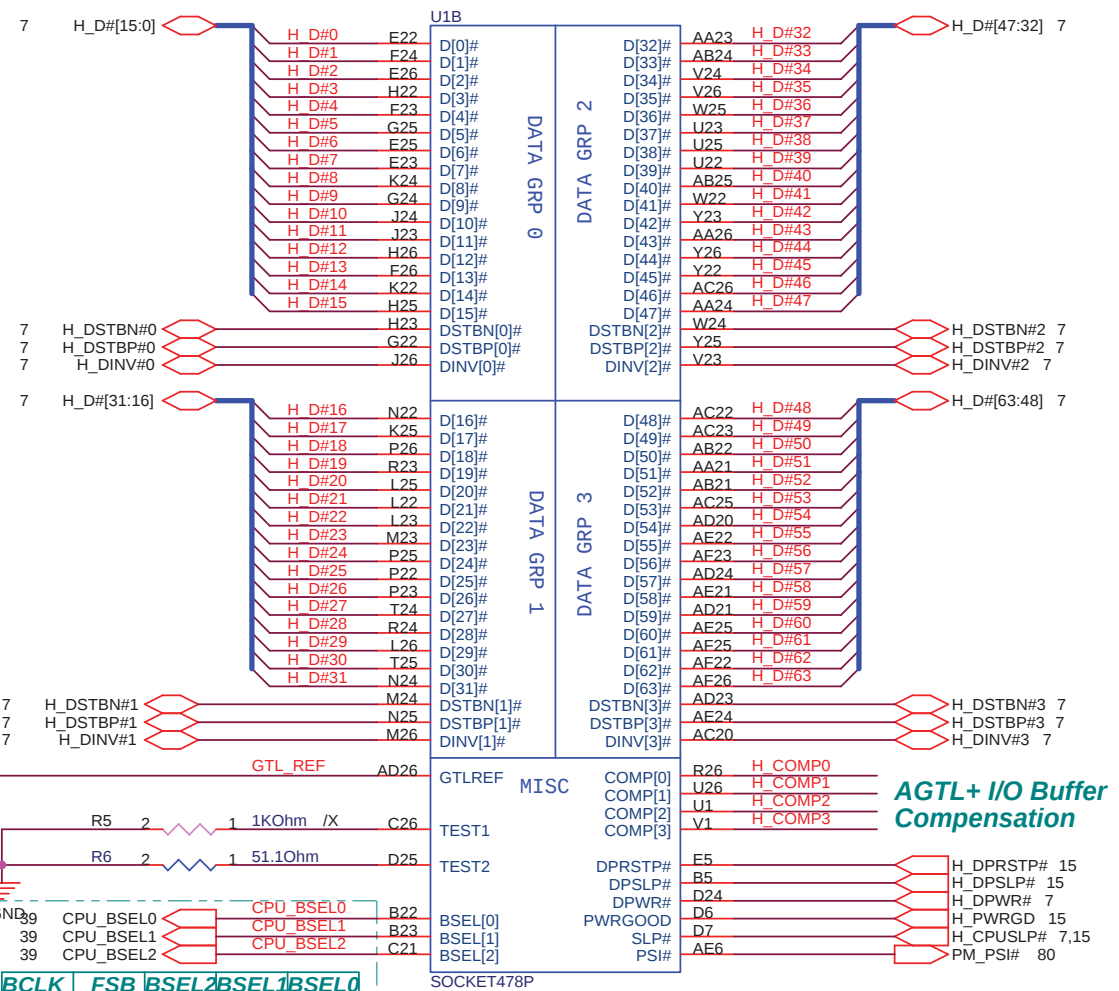
Default Strapping When Not Used



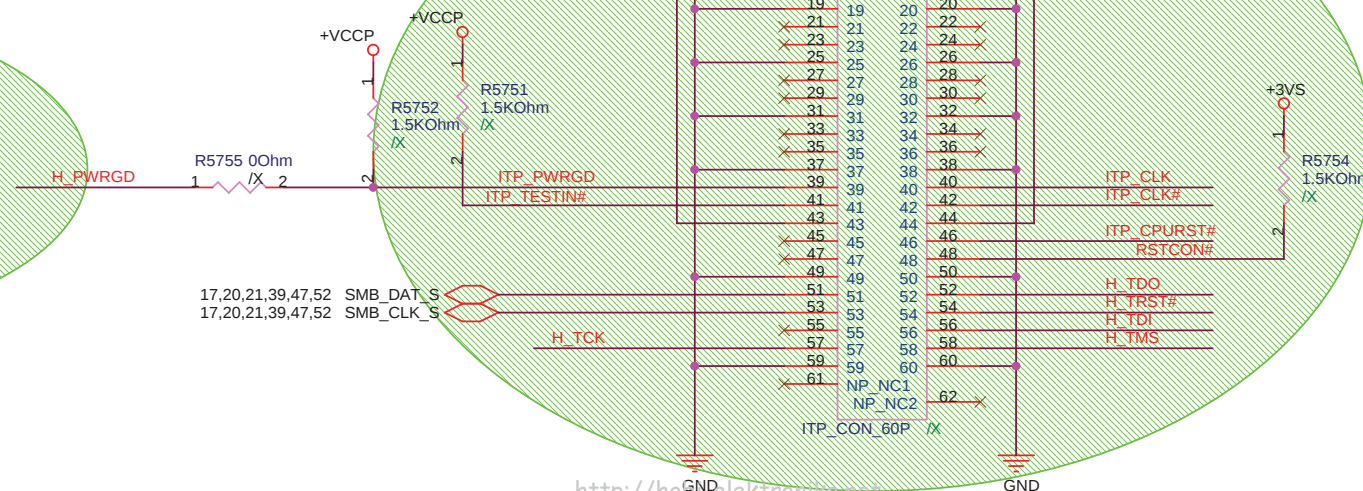
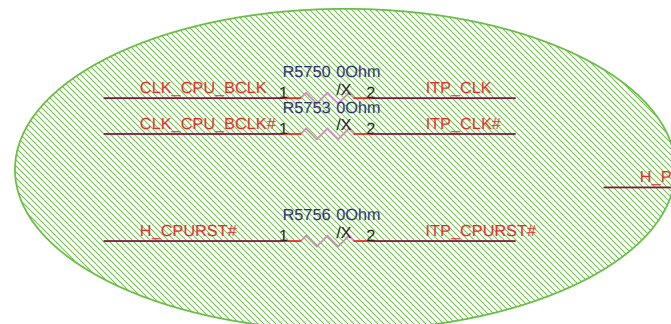
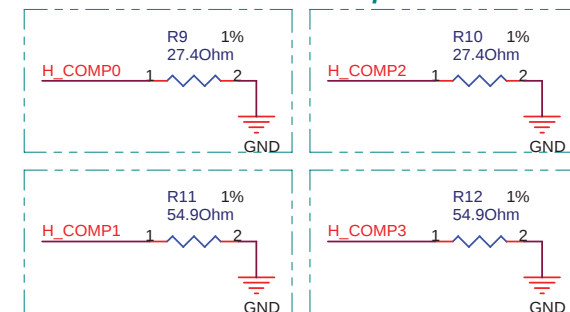
AGTL+ I/O Voltage Reference



BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H



AGTL+ I/O Buffer Compensation

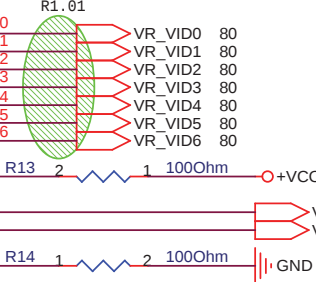
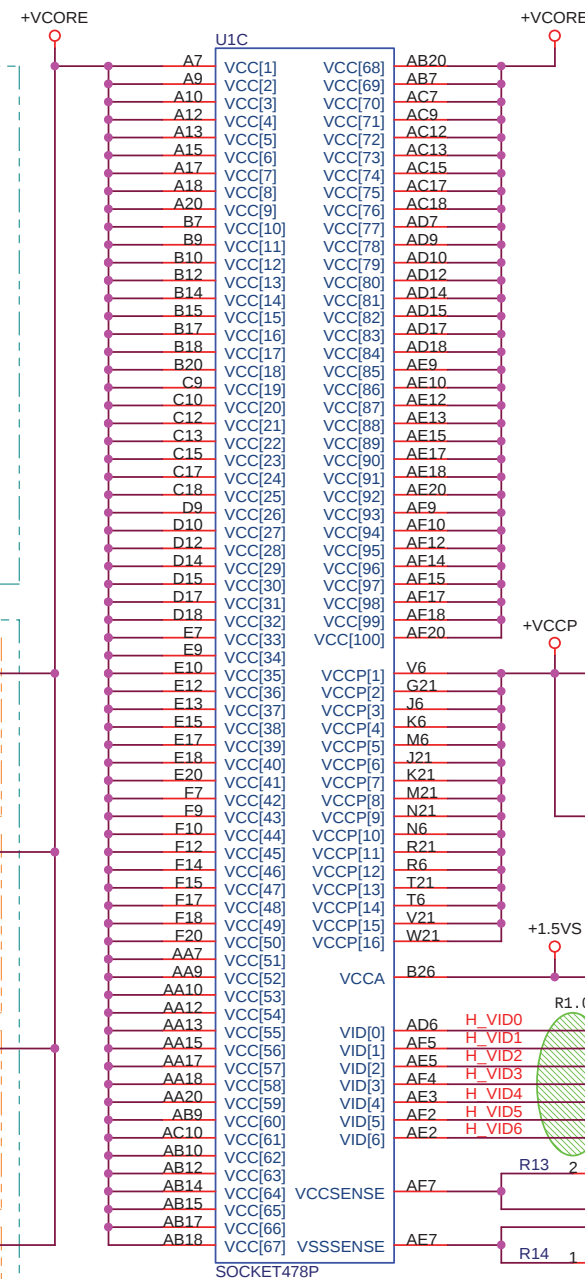
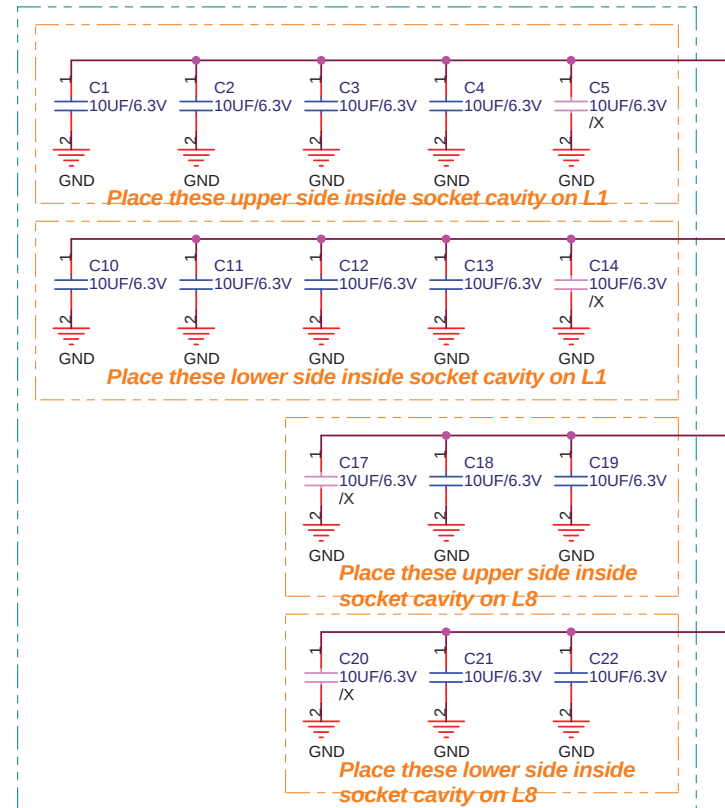


**CPU +VCORE
Bulk-Decoupling
Capacitors**

**CPU +VCORE
Mid-Frequency
Capacitors**

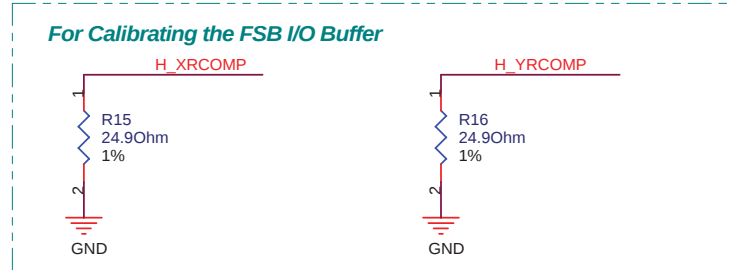
**CPU +VCCP
Decoupling
Capacitors**

**CPU +VCCA
Decoupling
Capacitors**

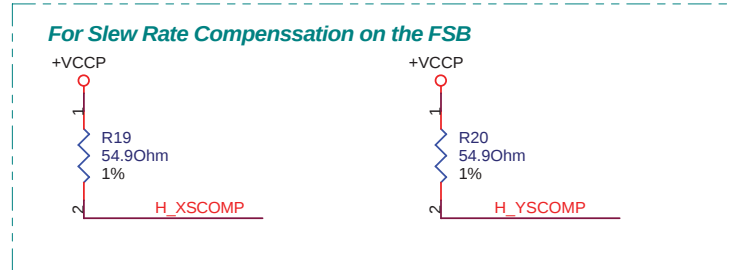


+VCCP Decoupling Capacitor
Intel: 270UF *1, 0.1UF *6
R1F: 220UF *1, 0.1UF *4

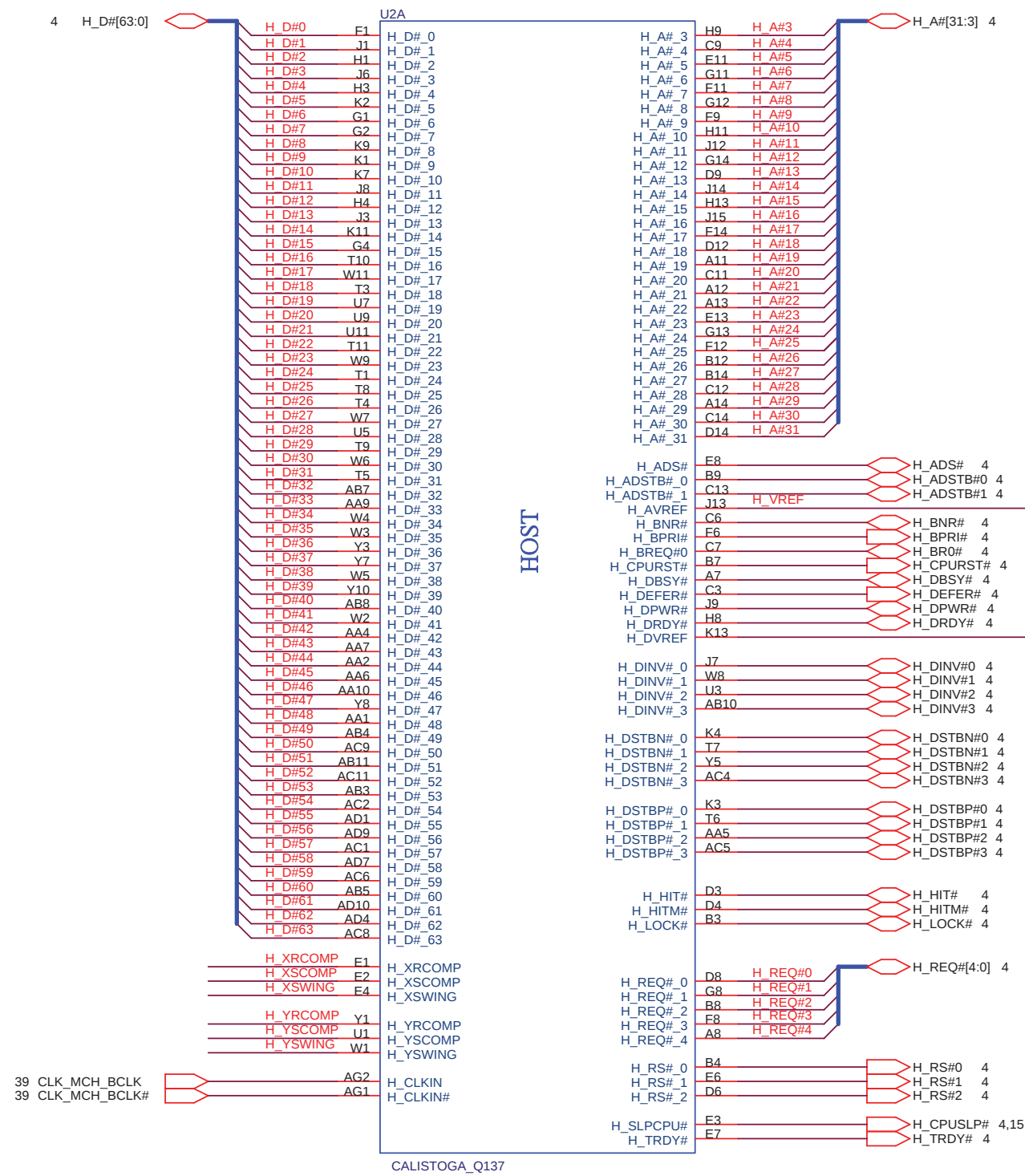
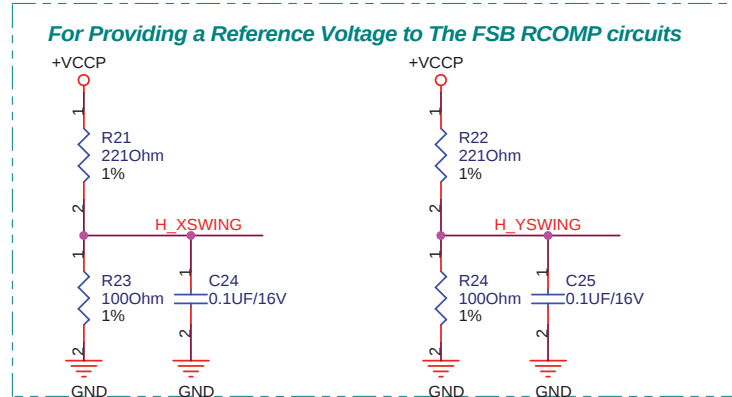
RCOMP



SCOMP



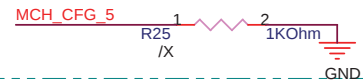
Voltage Swing



GMCH Strapping

CFG5 : DMI Strap

0 = DMI x2
1 = DMI x4 (D)

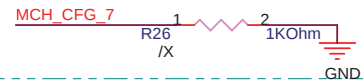


CFG[13:12] : GMCH Test Mode

00 = Partial CLK Gating Disable
01 = XOR Mode Enable
10 = All Z Mode Enable
11 = Normal Operation (D)

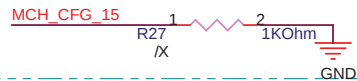
CFG7 : CPU Strap

0 = DT/Transpotable CPU
1 = Mobile CPU (D)



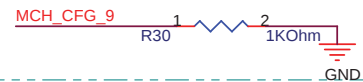
CFG15 : ICH RESET Disable

0 = ICH Reset Disable
1 = Normal Operation (D)



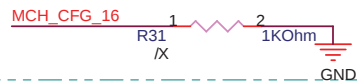
CFG9 : PCIE Graphic Lane

0 = Reverse Lane
1 = Normal Operation (D)



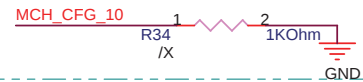
CFG16 : FSB Dynamic ODT

0 = Dynamic ODT Disable
1 = Dynamic ODT Enable (D)



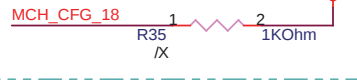
CFG10 : HOST PLL VCO Select

0 = Reserved
1 = Mobility (D)



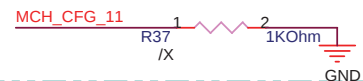
CFG18 : VCC Select

0 = 1.05V (D)
1 = 1.5V



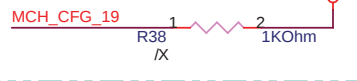
CFG11 : PSB 4x CLK Enable

0 = 4x Enable
1 = 8x Enable (D)



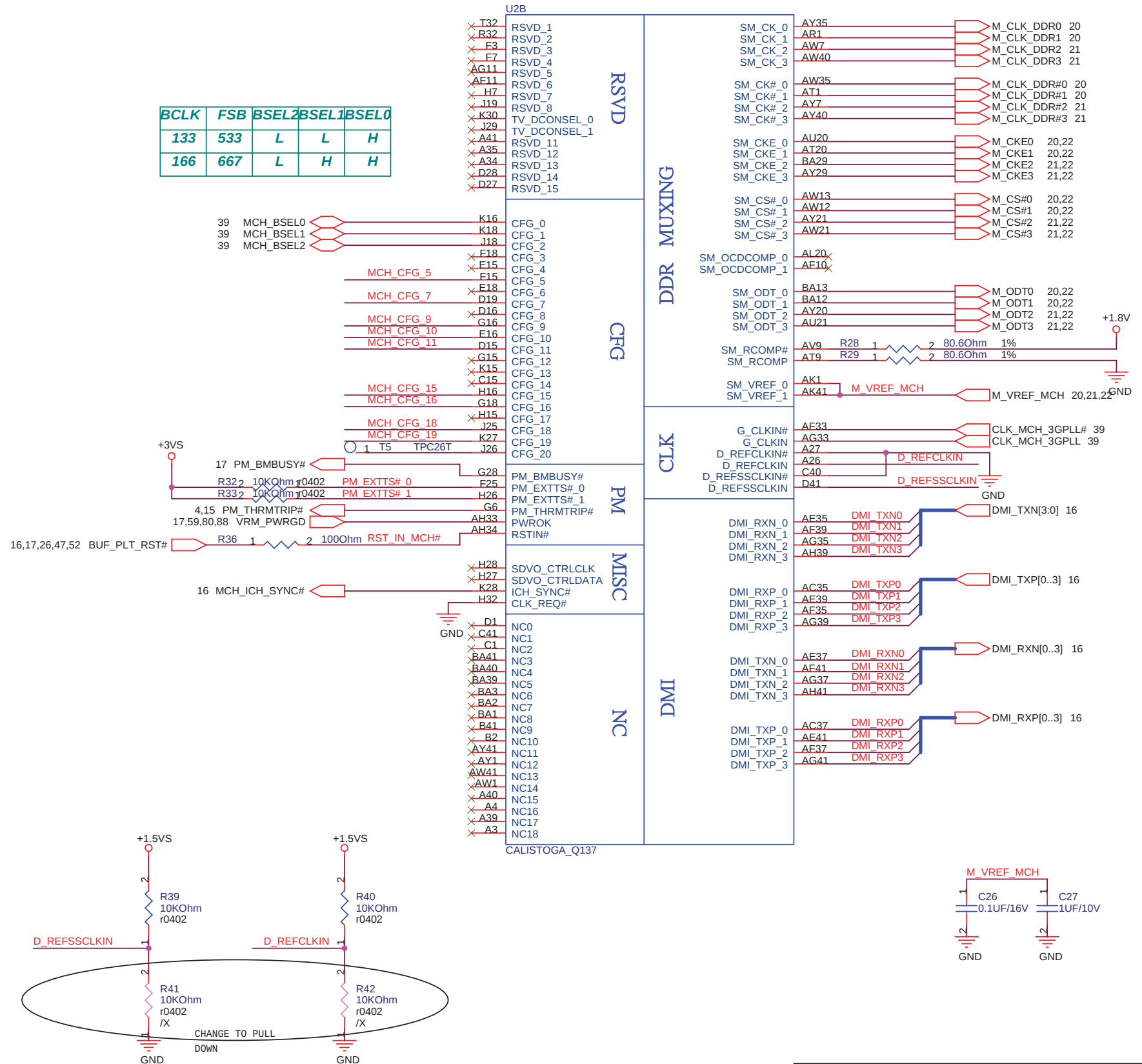
CFG19 : DMI Lane Reversal

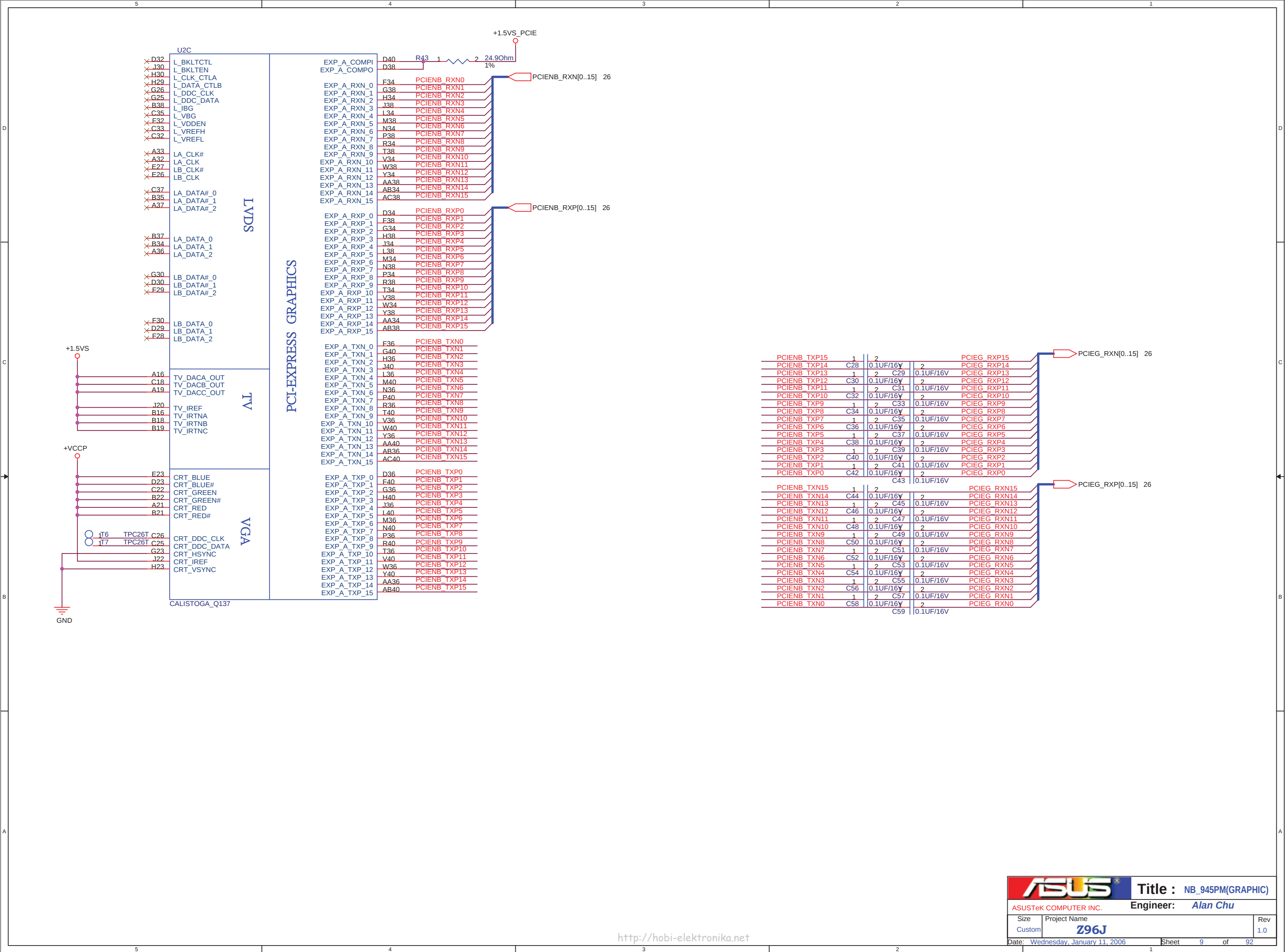
0 = Normal Operation (D)
1 = Lanes Reversed

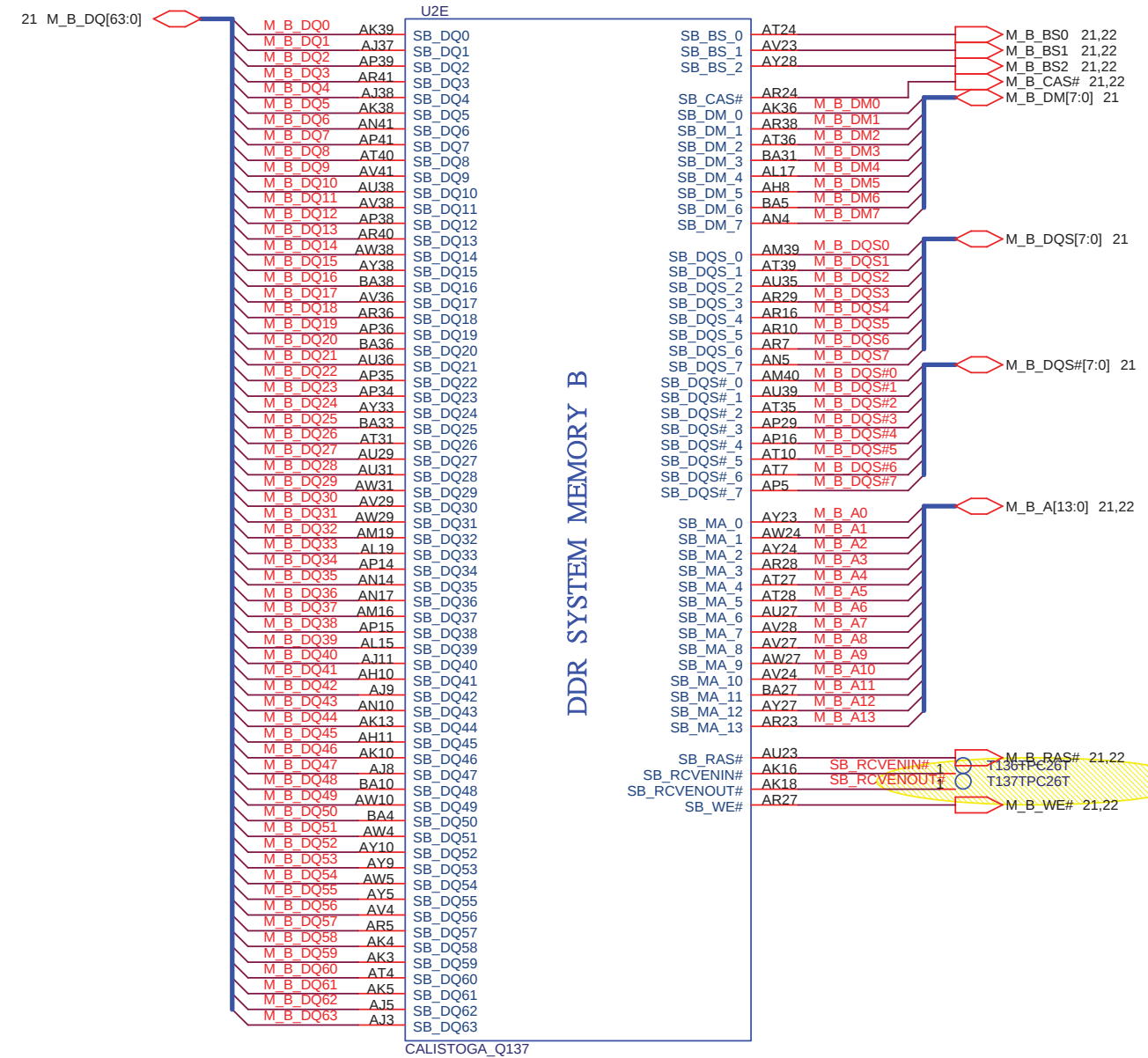
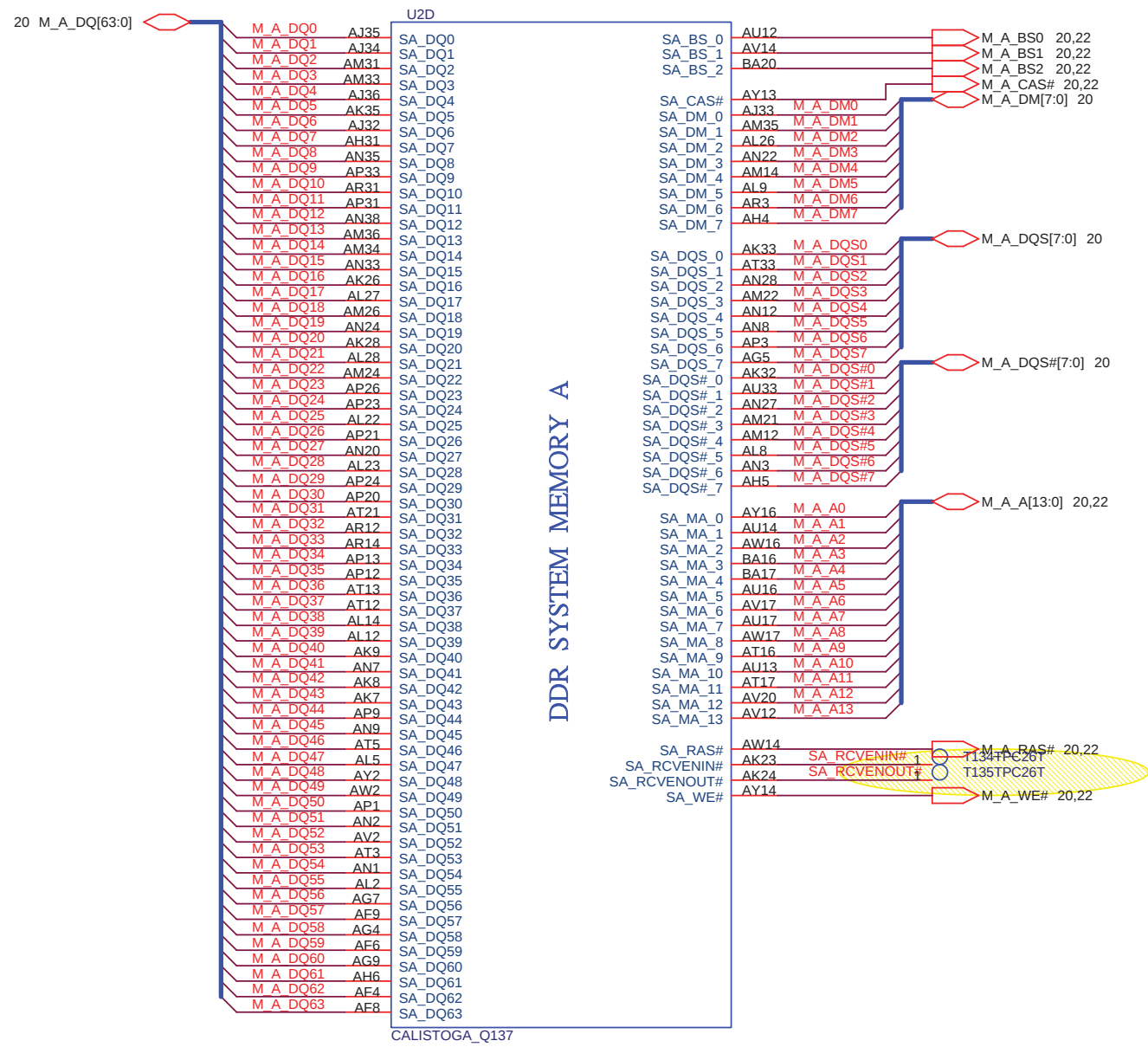


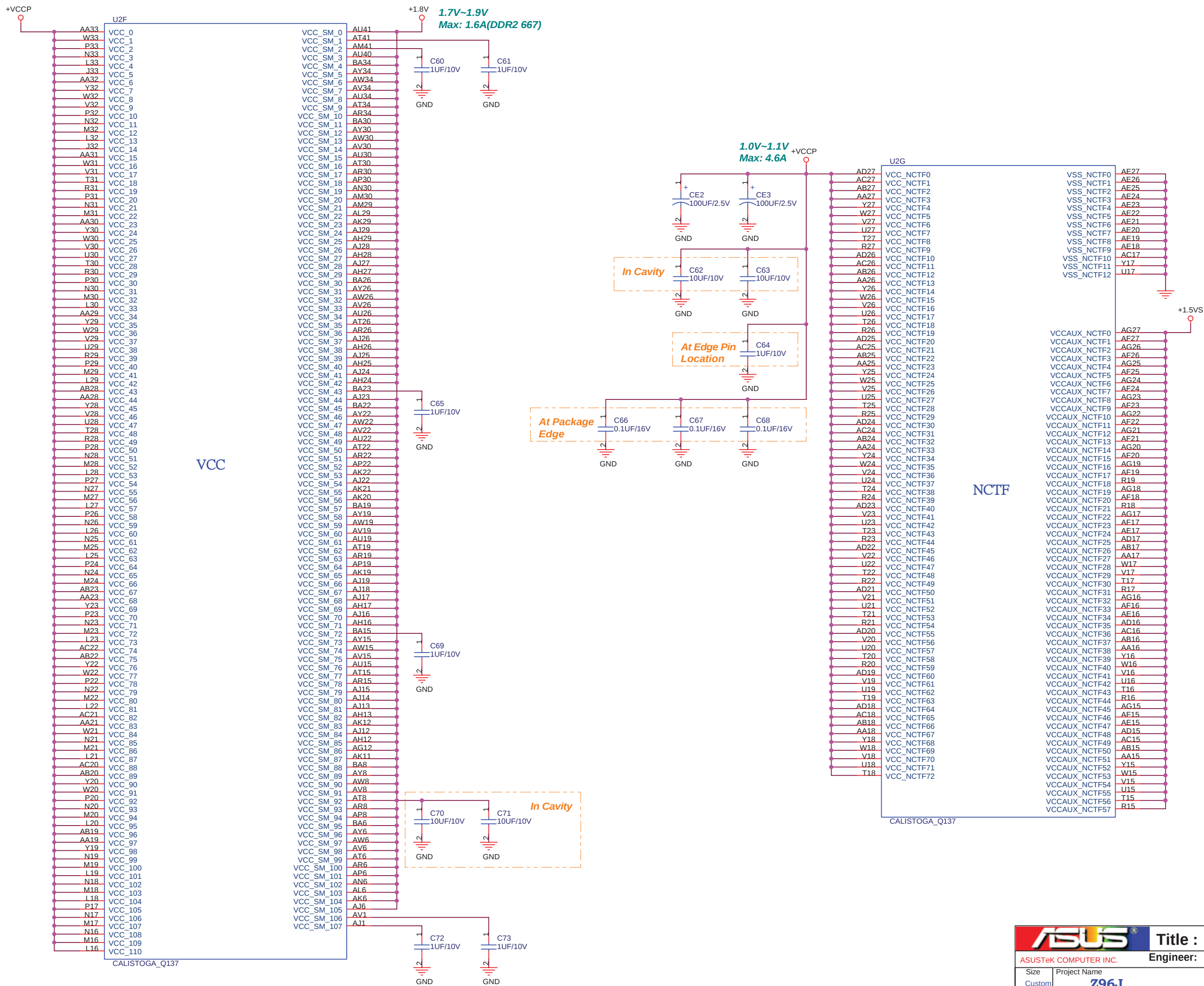
Note: CFG[17:3] have internal pull-up while CFG[20:18] have internal pull-down.

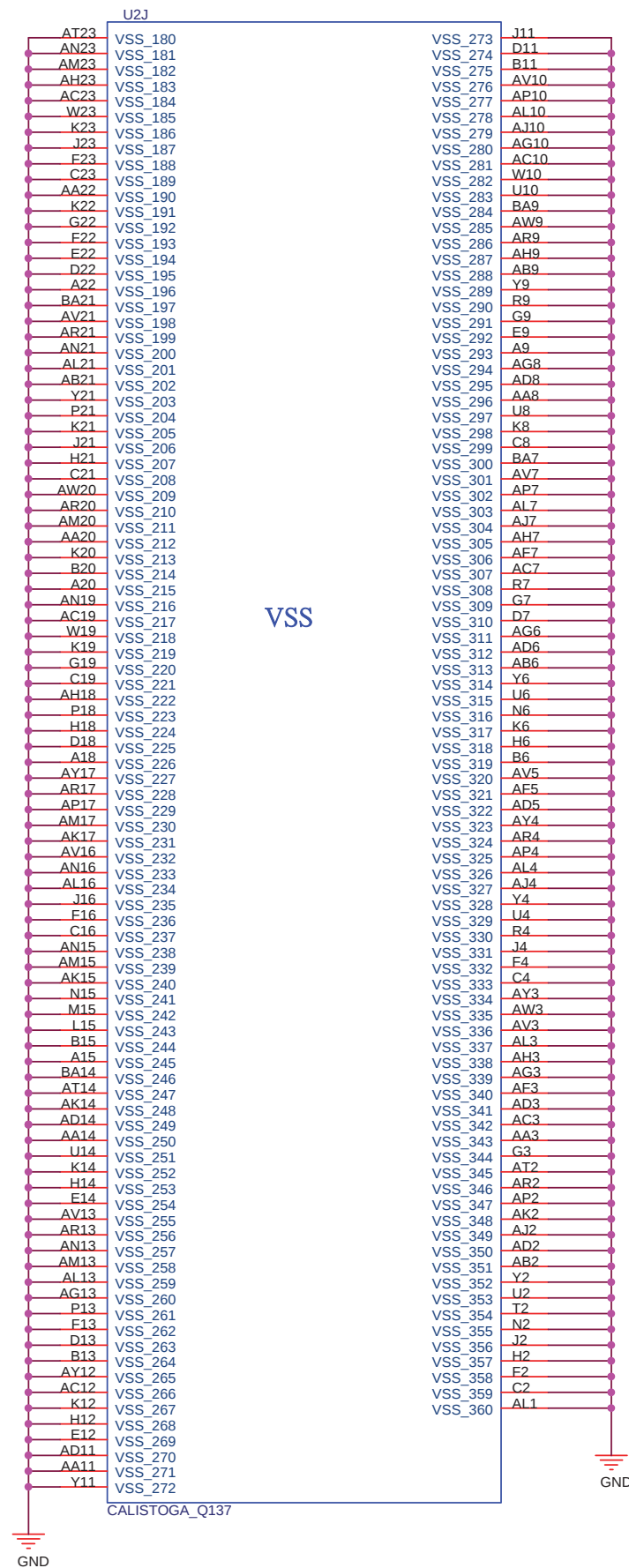
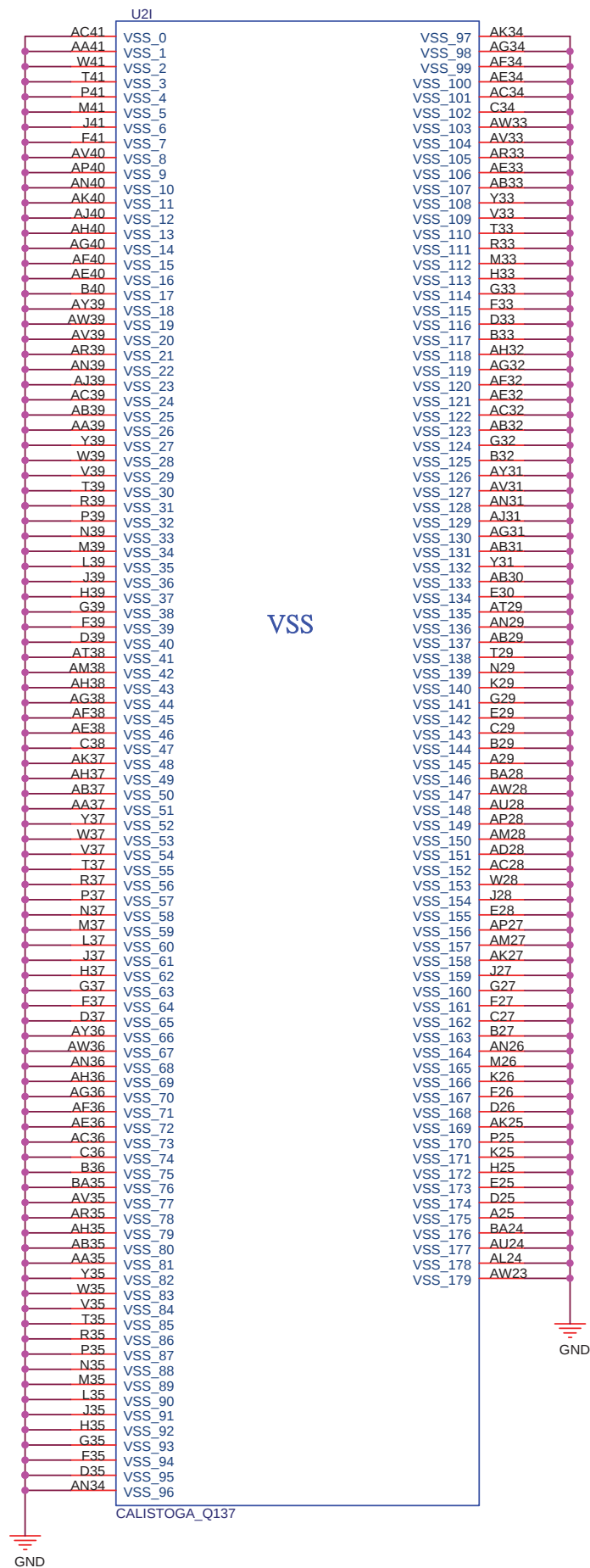
BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

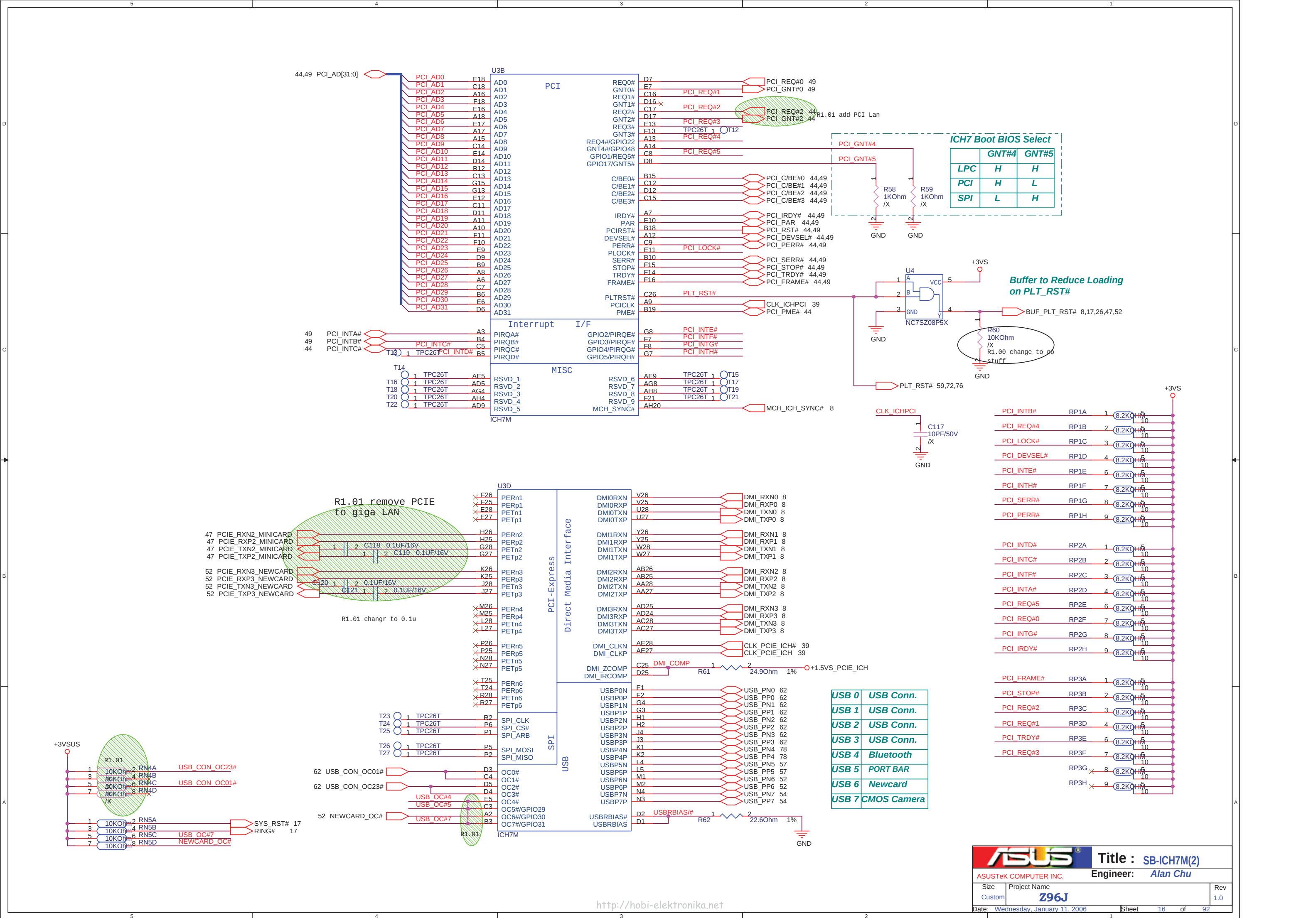




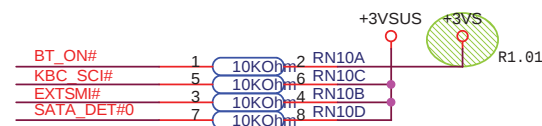
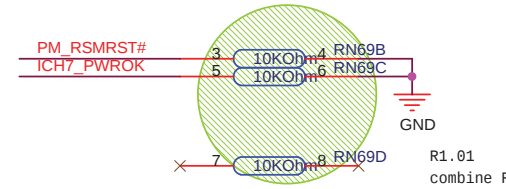
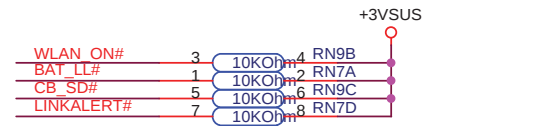
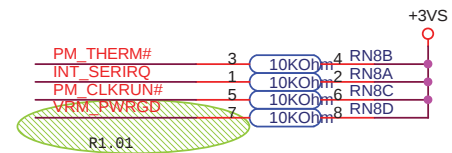
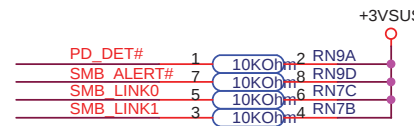
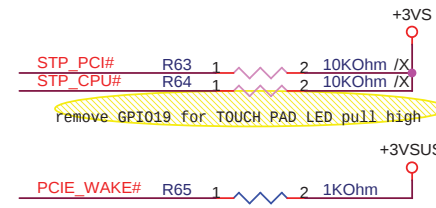
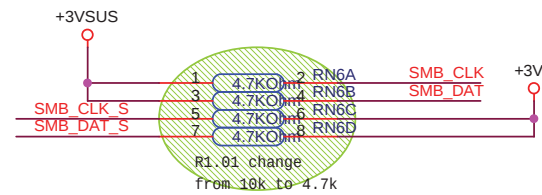
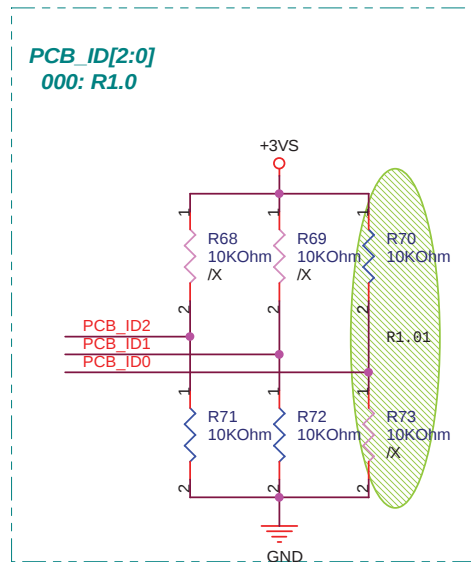
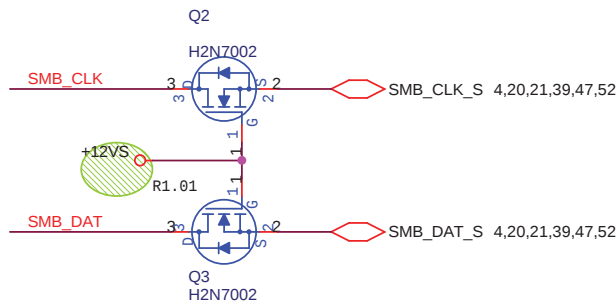
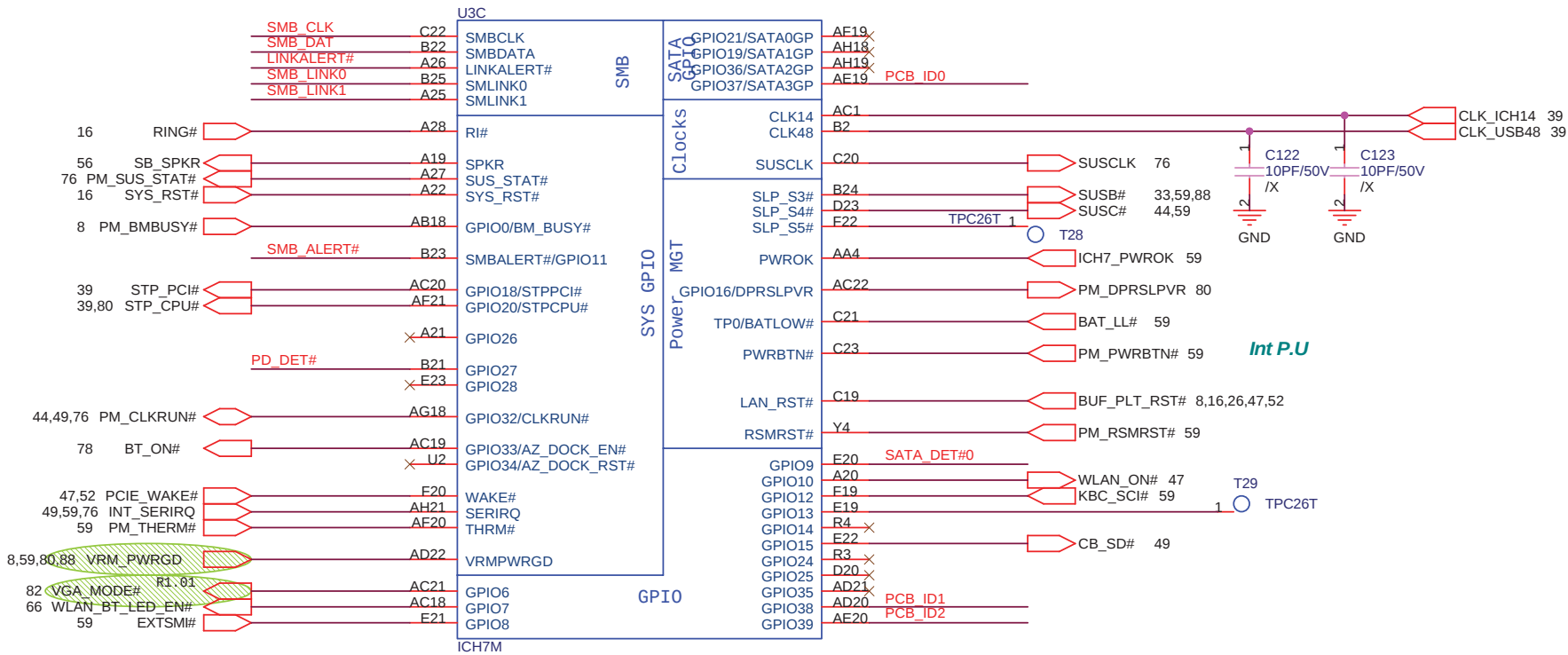


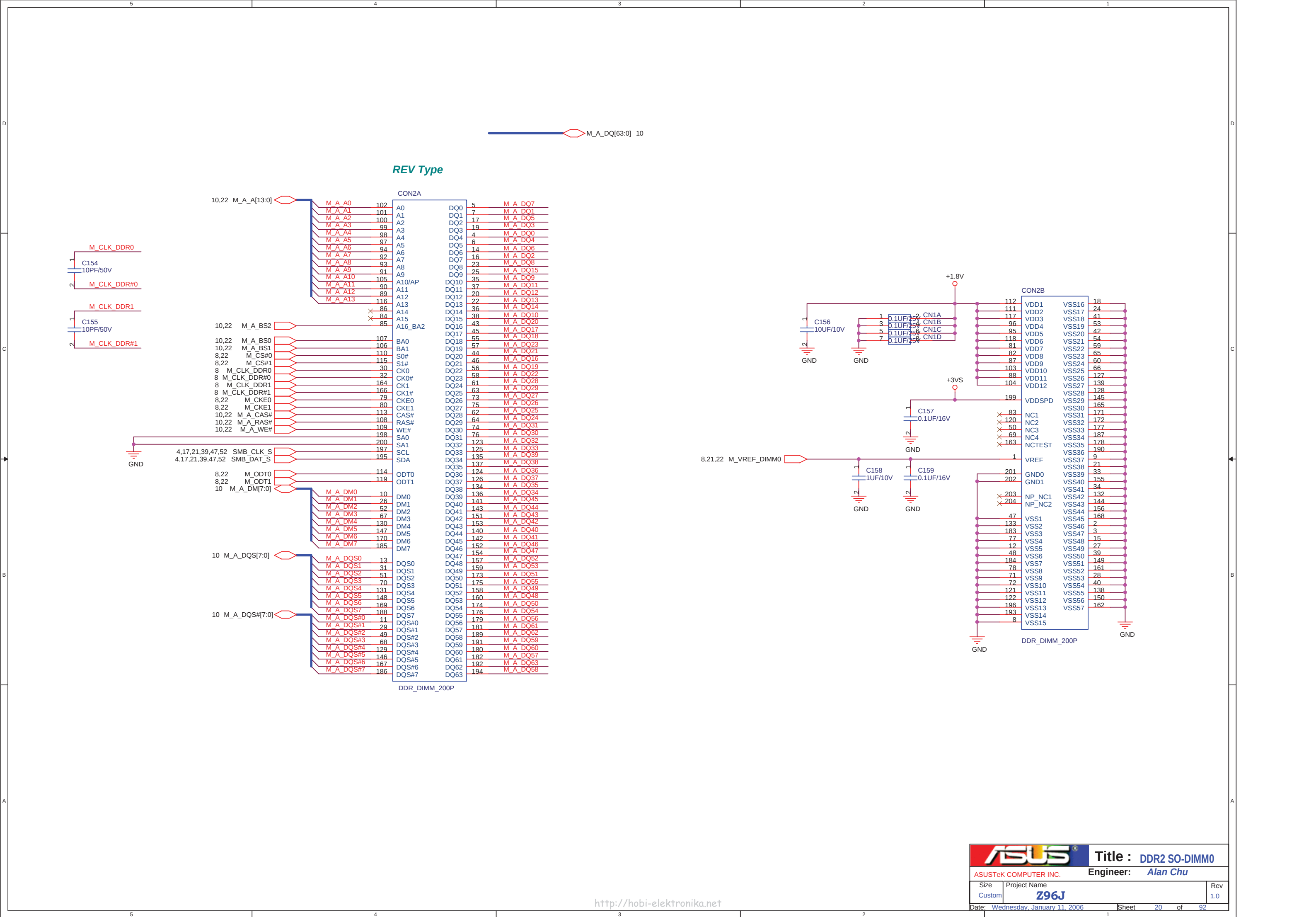


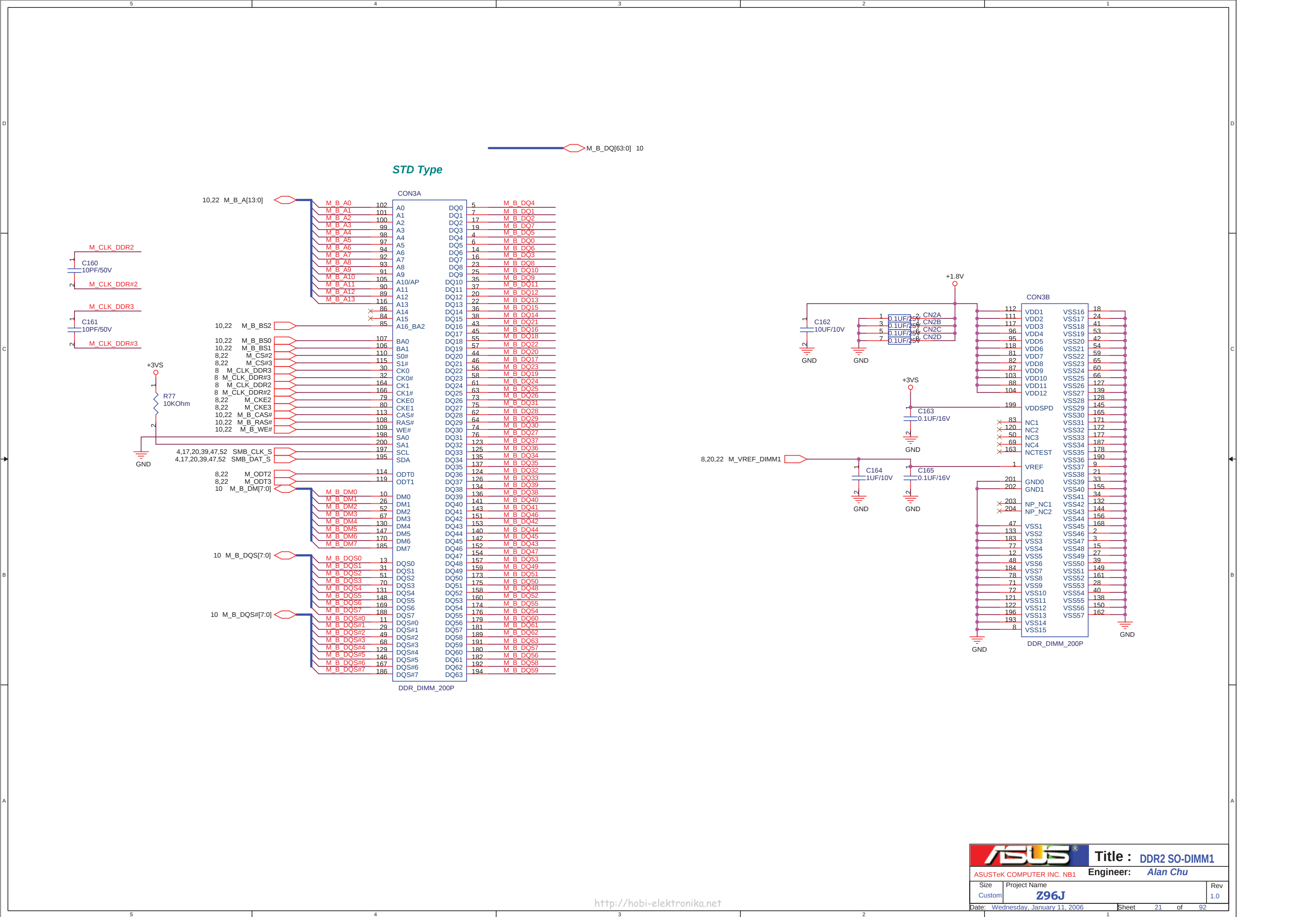


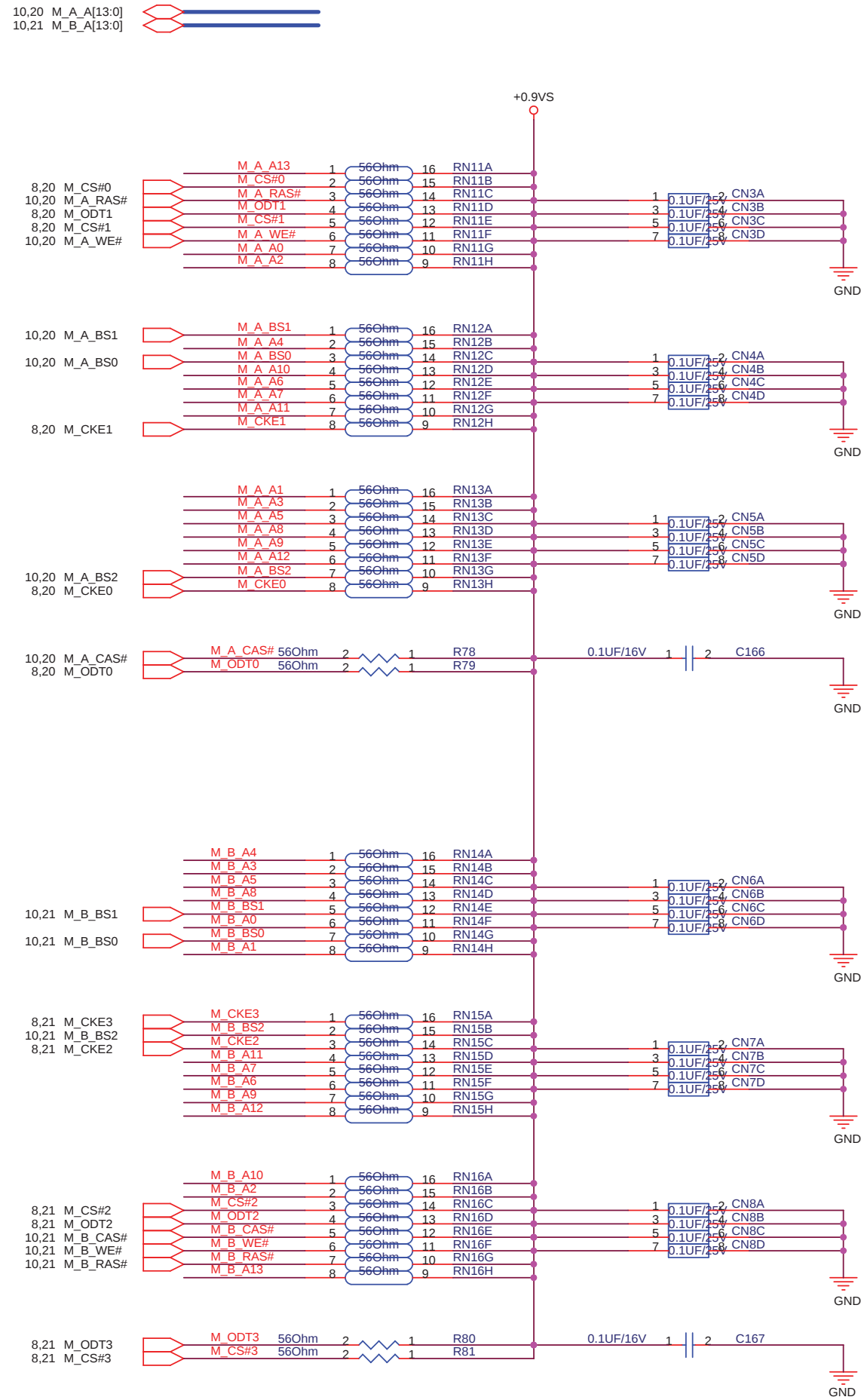
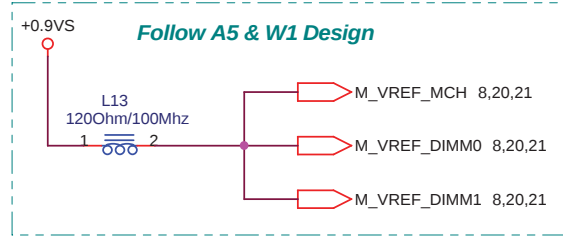


R1.01 add VGA mode select
GPU_VID = 1; Battery Mode ; +1.15VO = 1.055V
GPU_VID = 0; Performance Mode ; +1.15VO = 1.158V

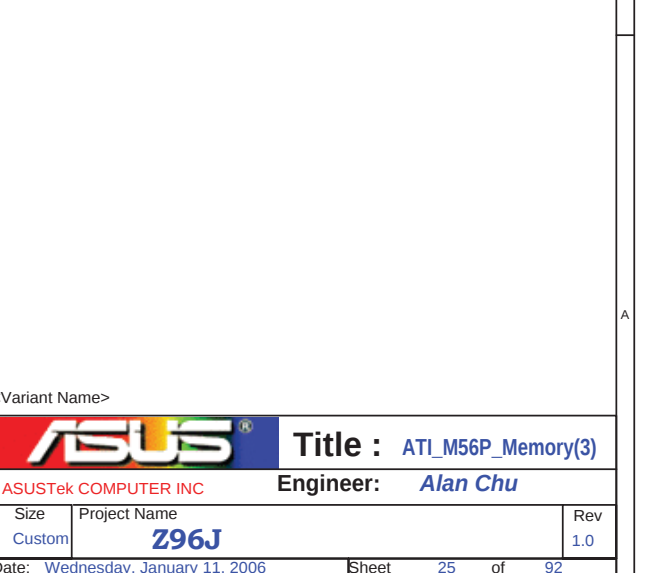
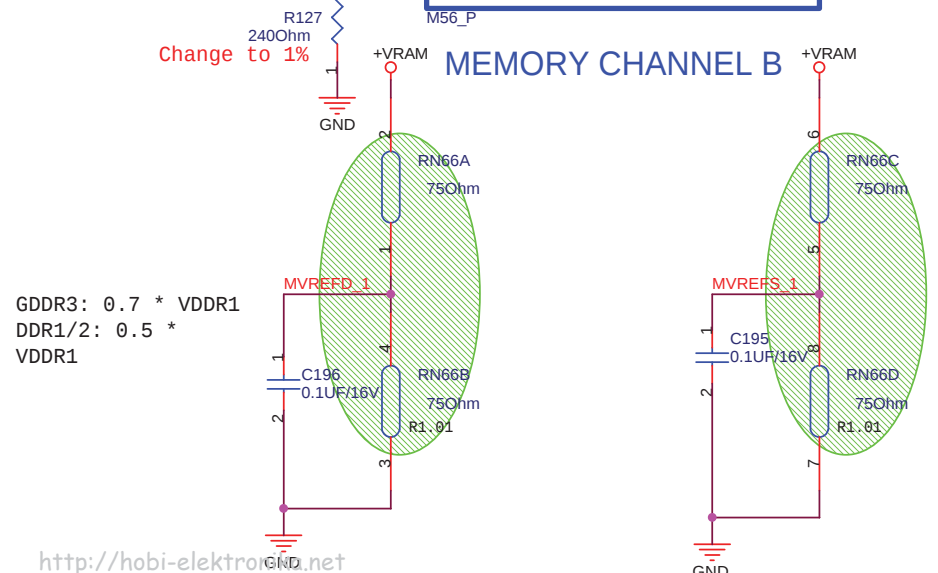
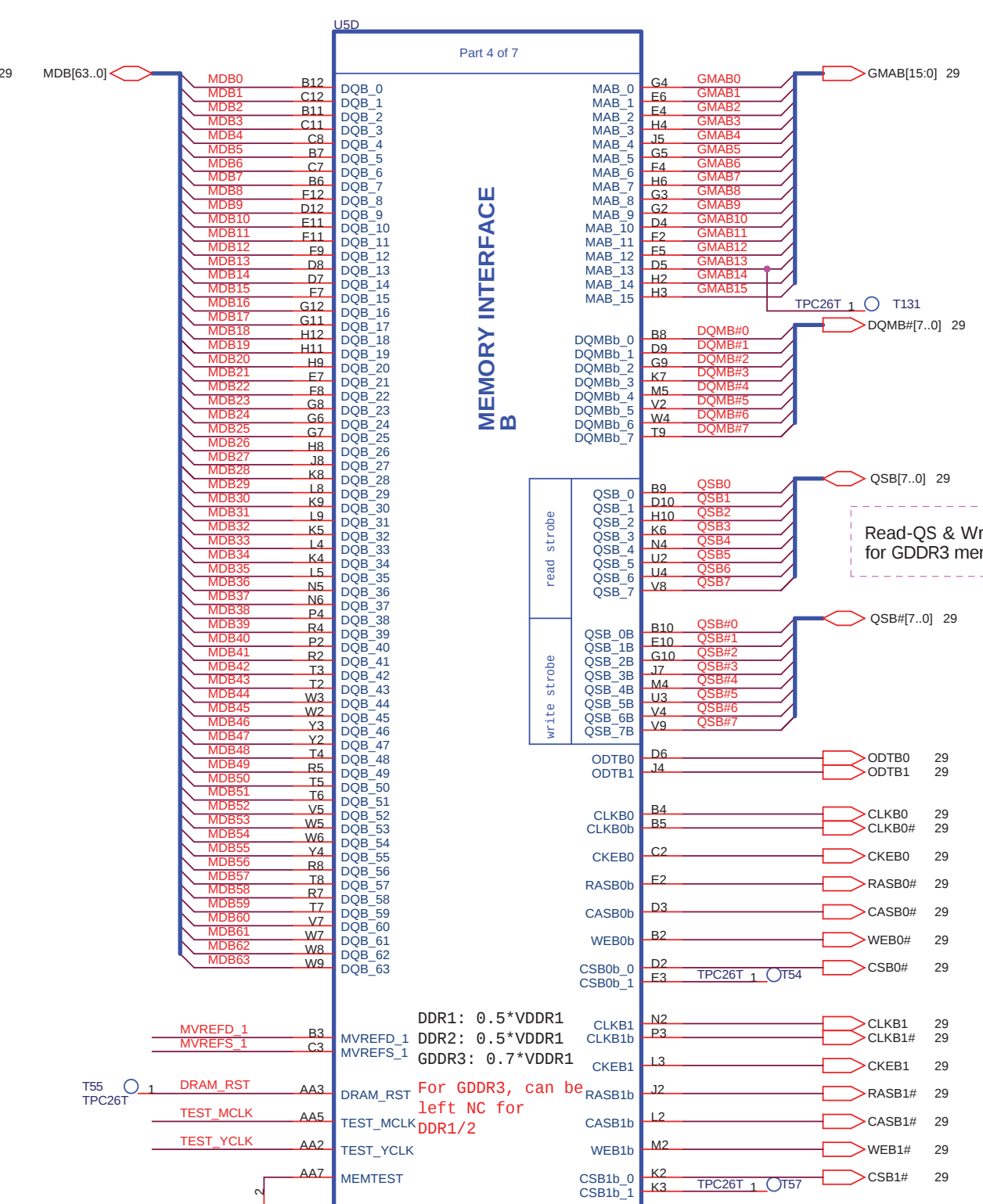
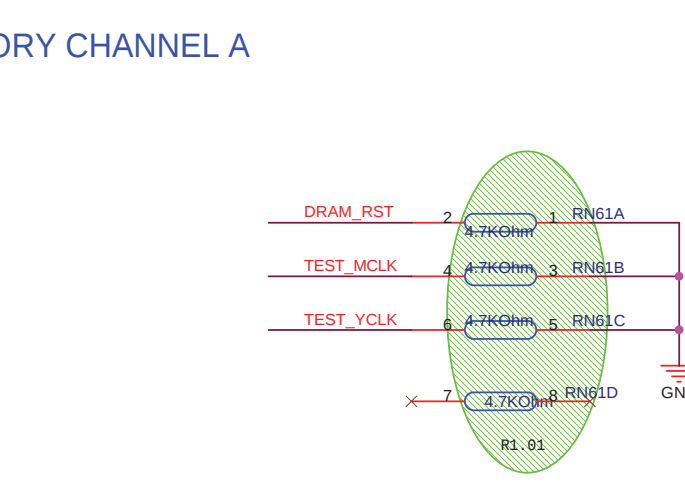
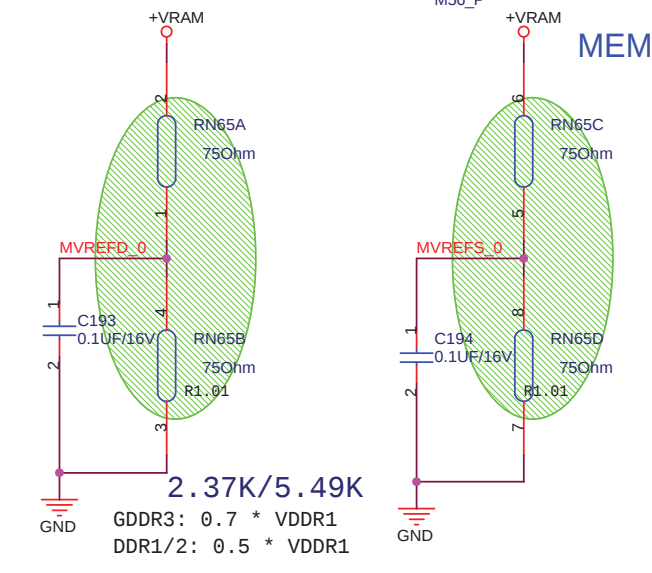
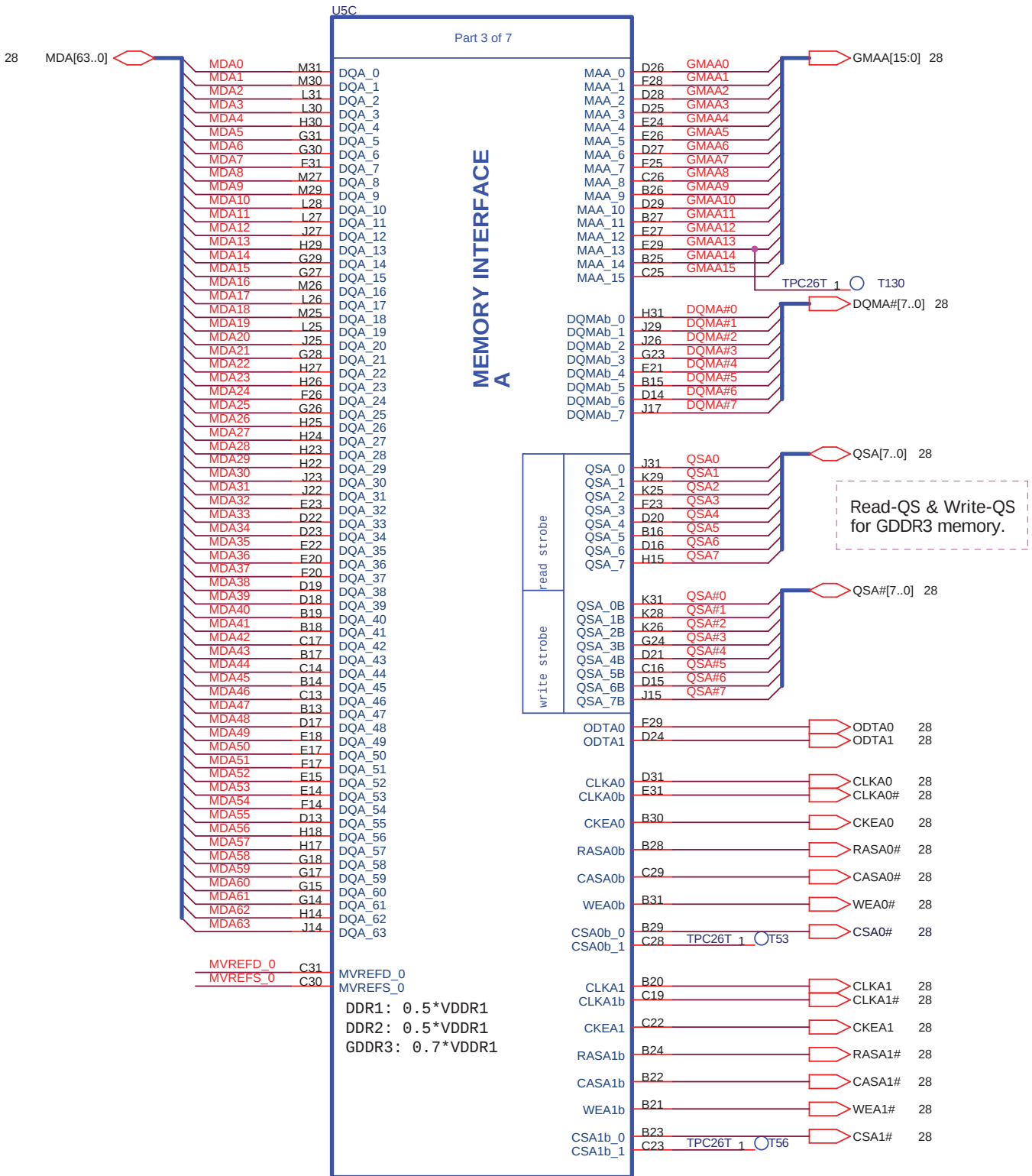












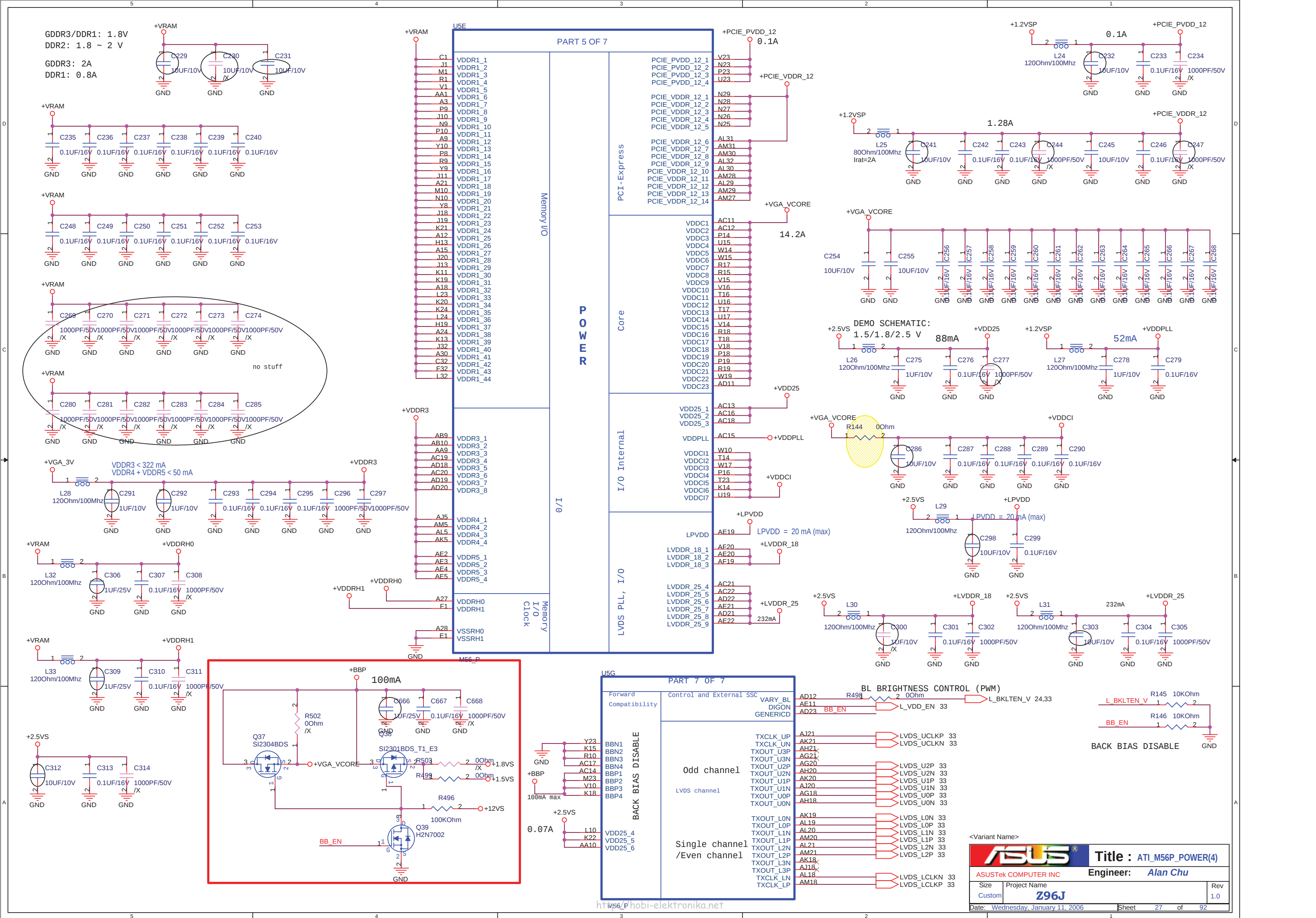
<Variant Name>

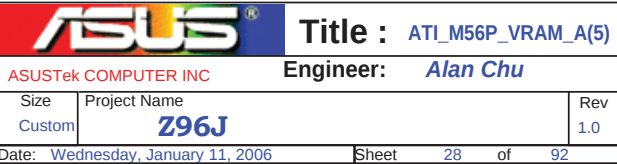
ASUS Title : **ATI_M56P_Memory(3)**

ASUSTek COMPUTER INC Engineer: **Alan Chu**

Size	Project Name	Rev
Custom	Z96J	1.0

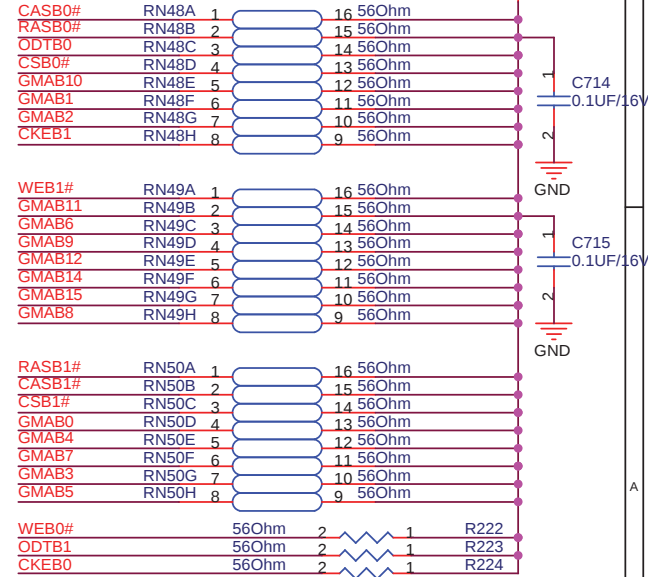
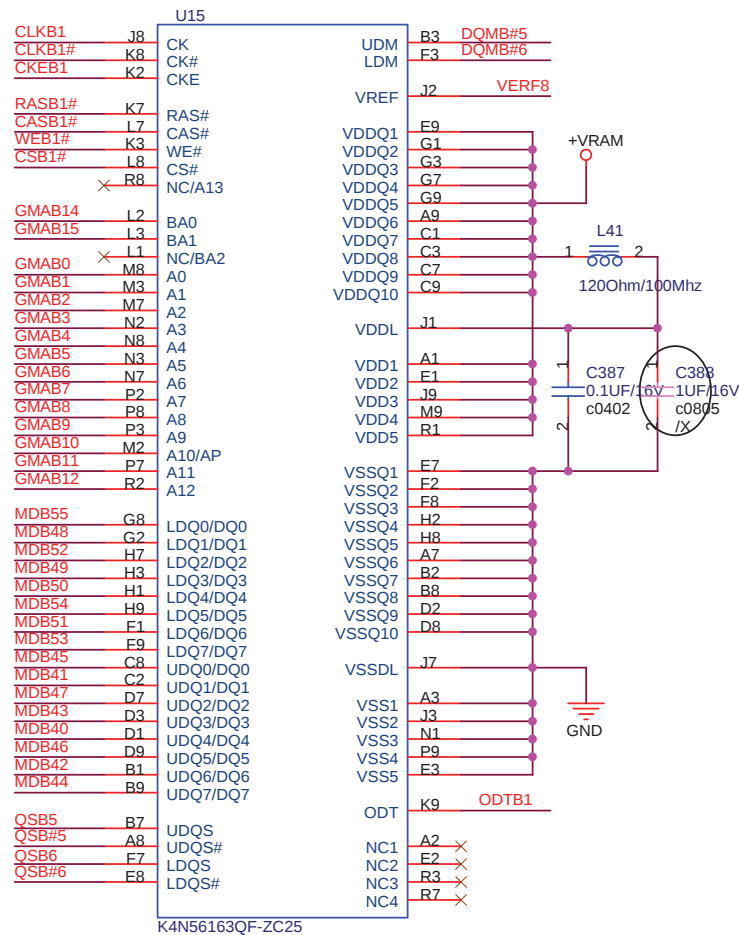
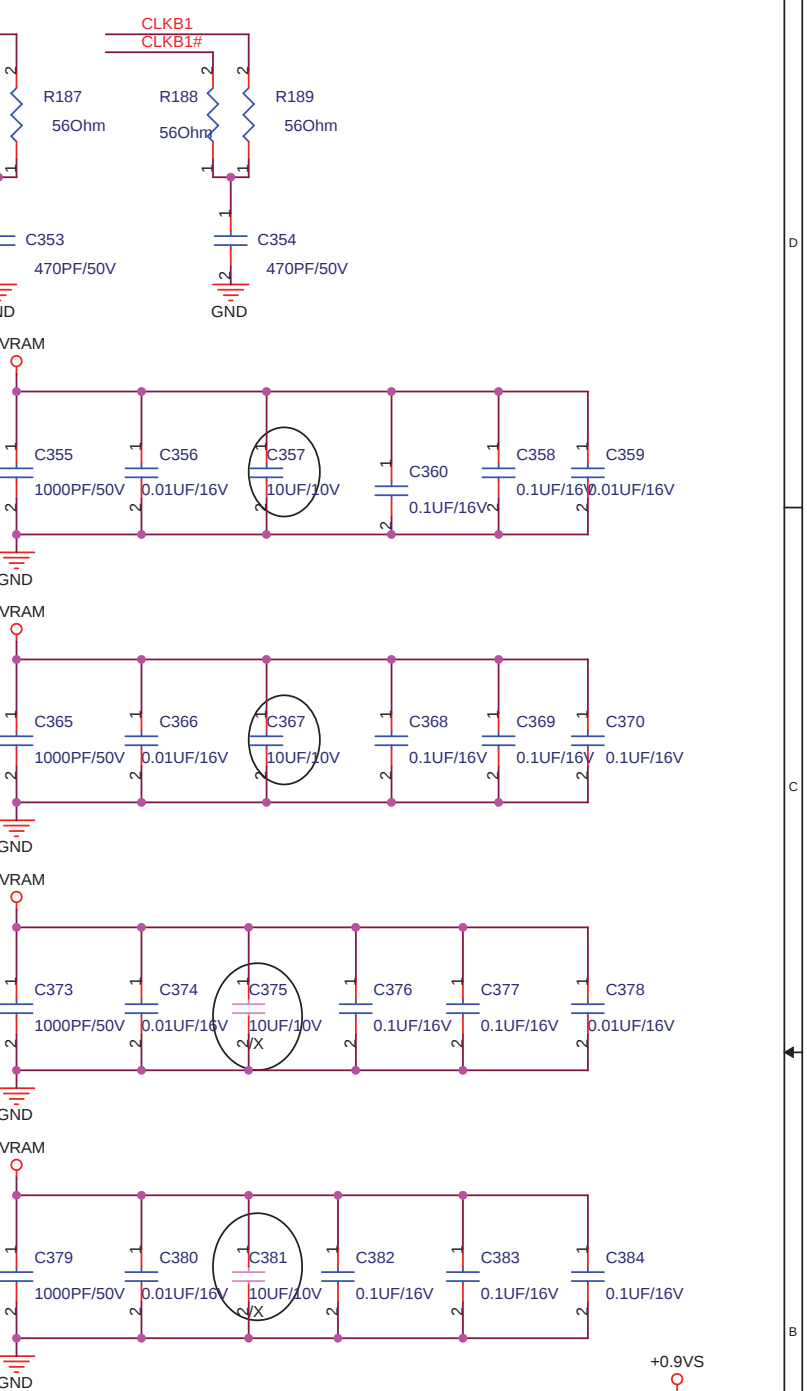
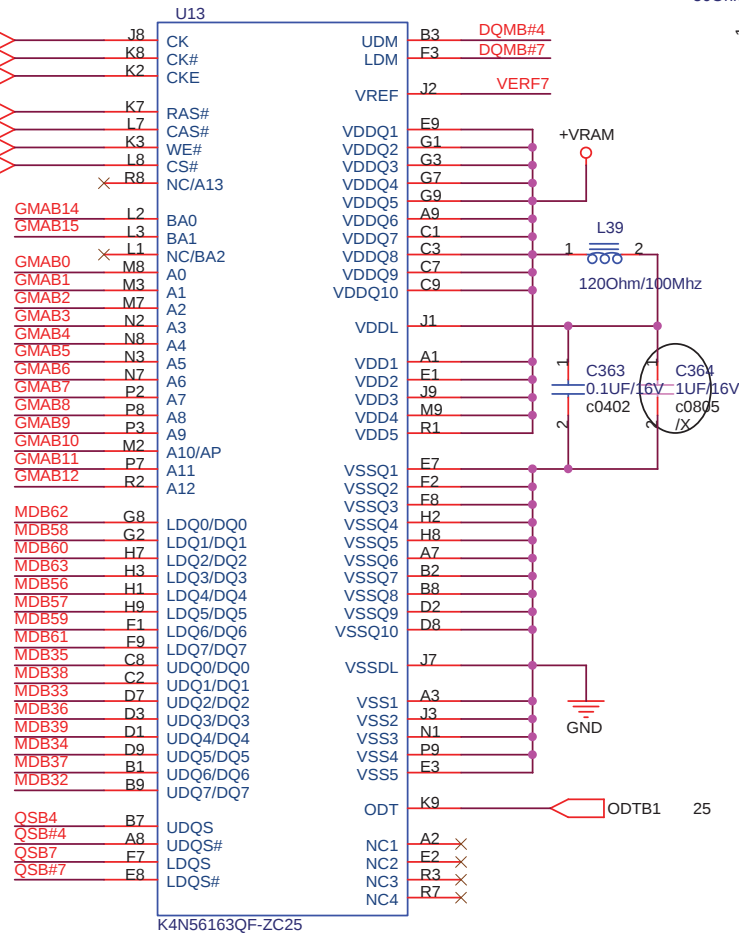
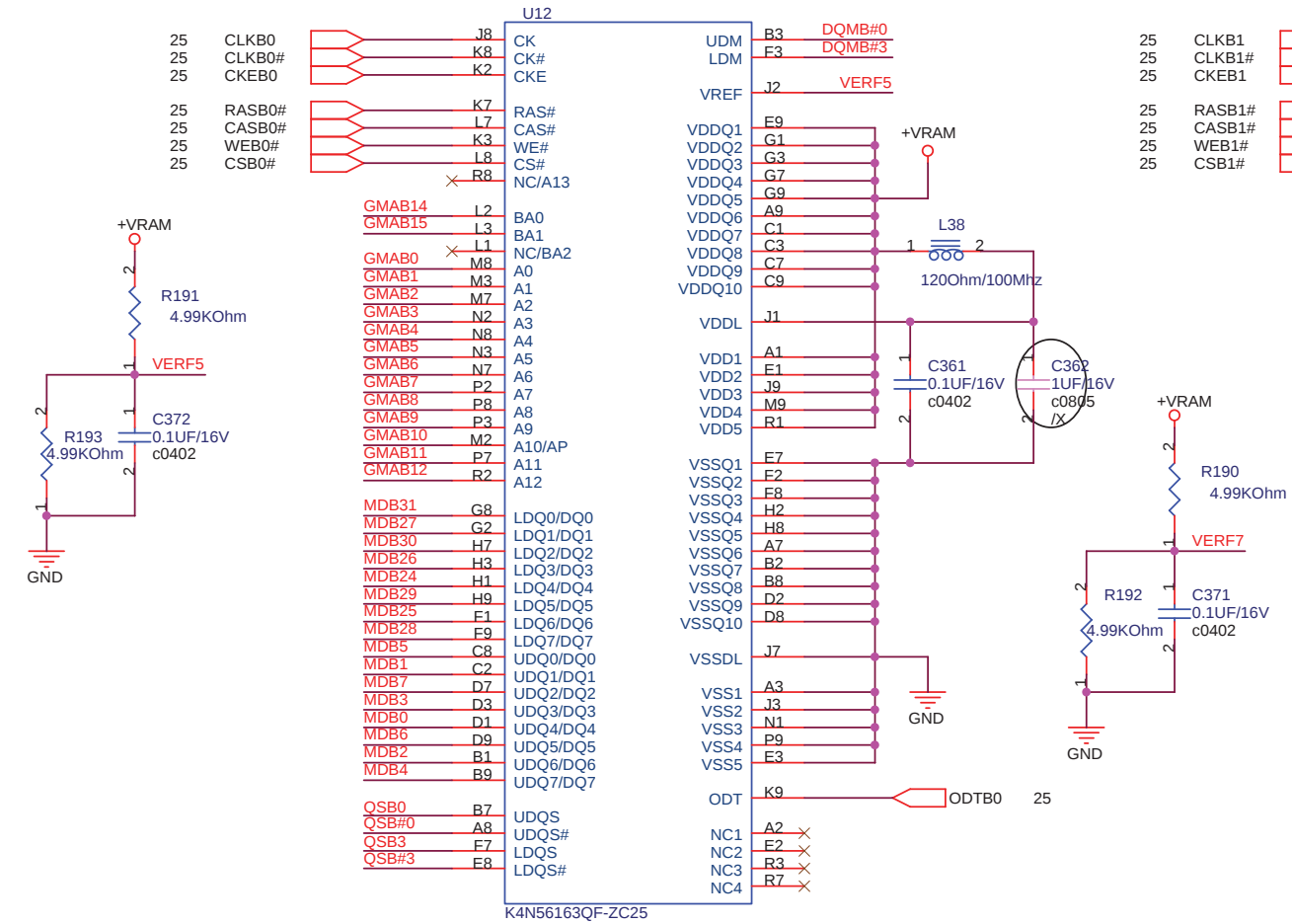
Date: Wednesday, January 11, 2006 Sheet 25 of 92

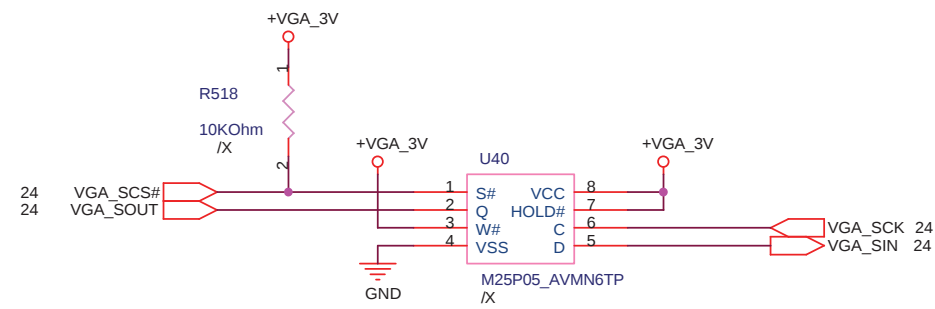


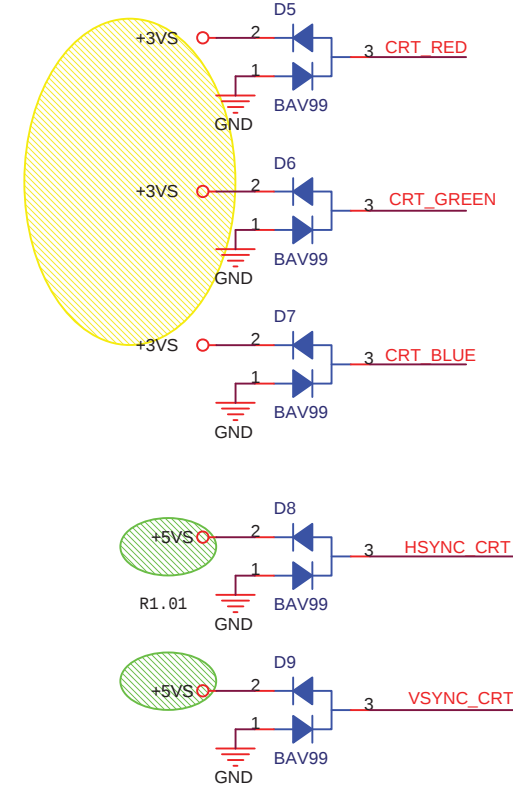
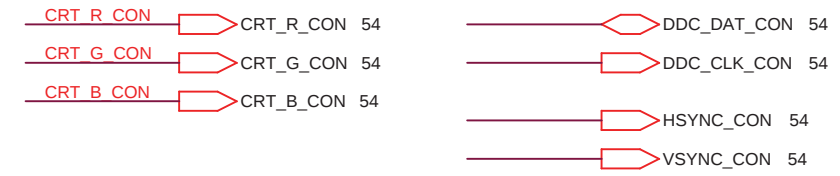
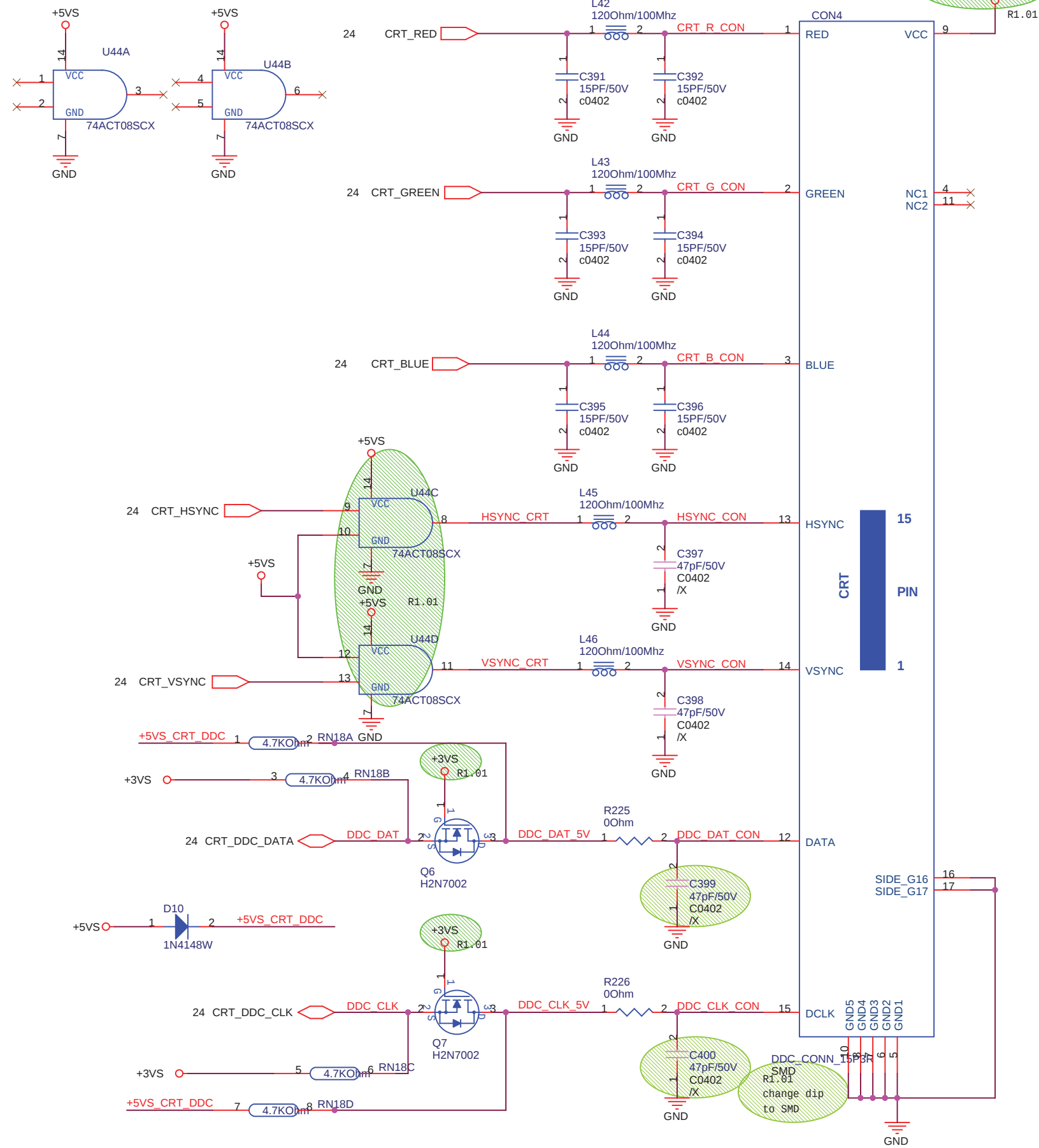


25 GMAB[15..0]
25 QSB[7..0]
25 QSB#[7..0]
25 DQMB#[7..0]

MDB[31..0] 25
MDB[63..32] 25







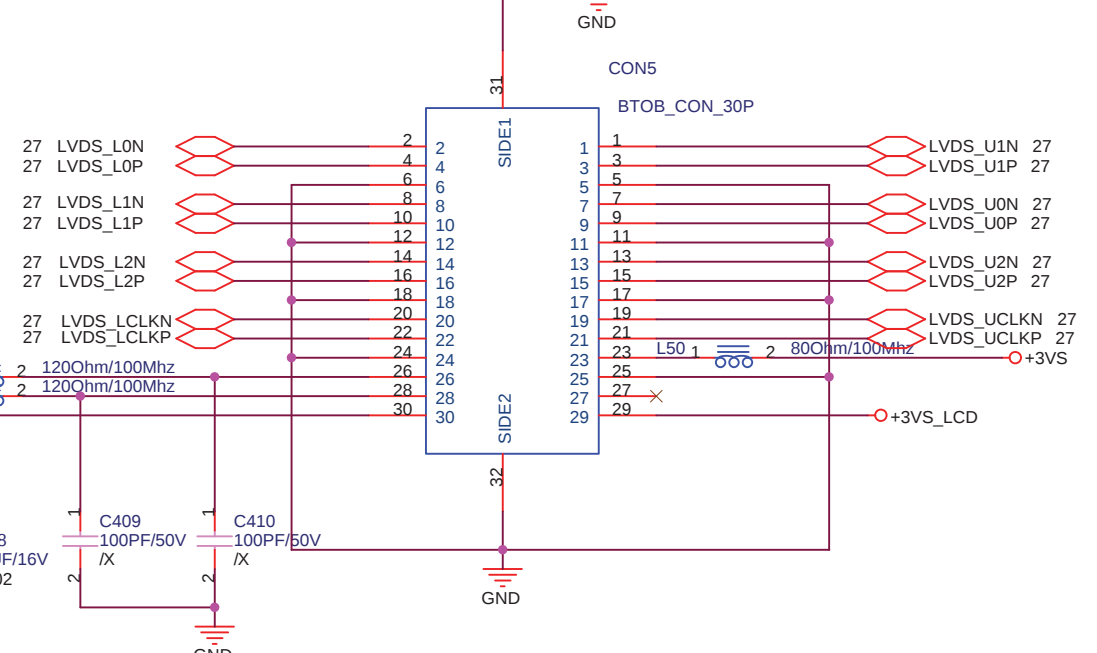
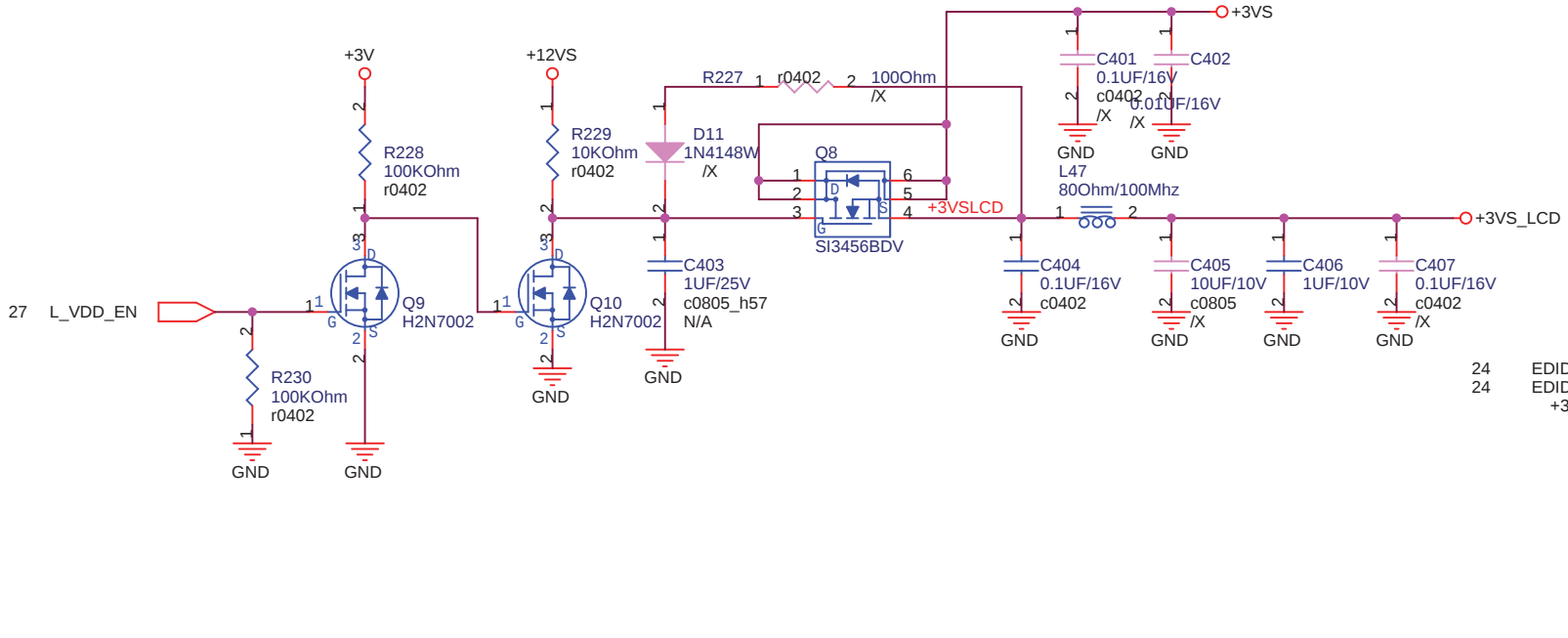
PLACE ESD Diodes near VGA port

ASUS		Title : CRT	
ASUSTeK COMPUTER INC		Engineer: Alan Chu	
Size	Project Name	Z96J	Rev 1.0
Custom			
Date: Wednesday, January 11, 2006		Sheet 32	of 92

LCD Backlight Control

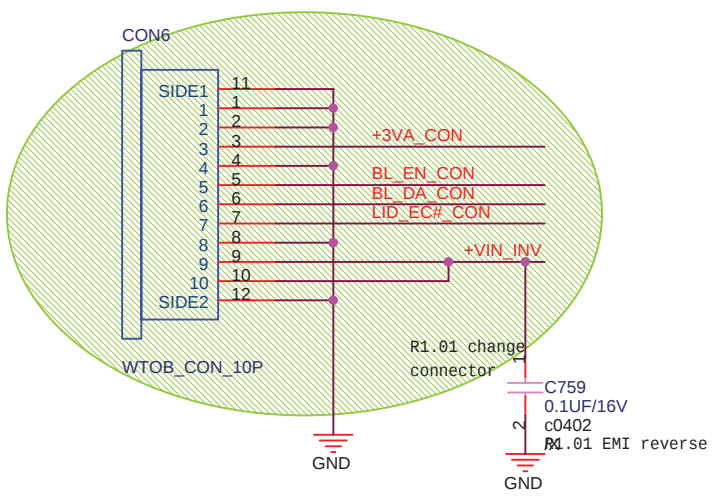
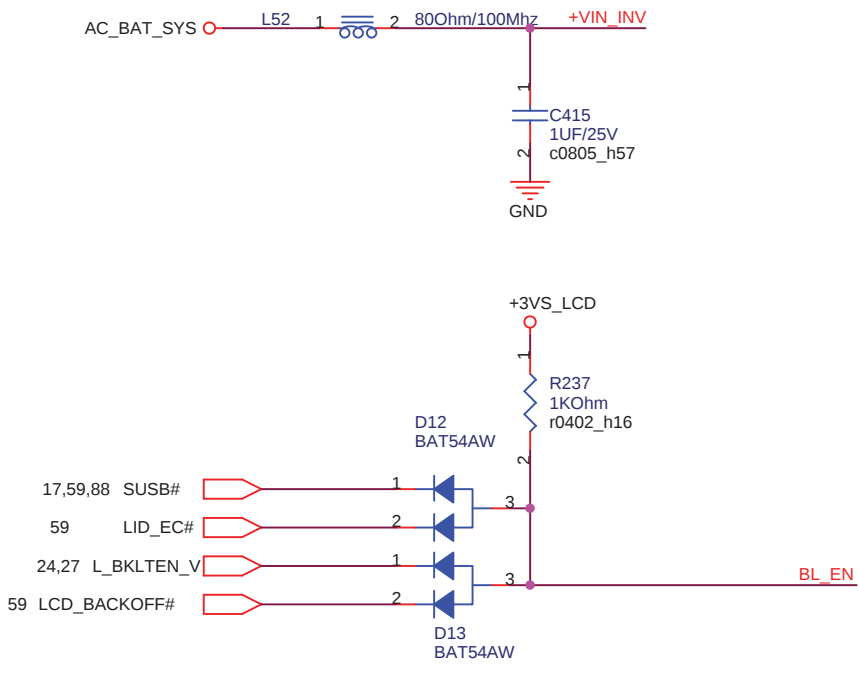
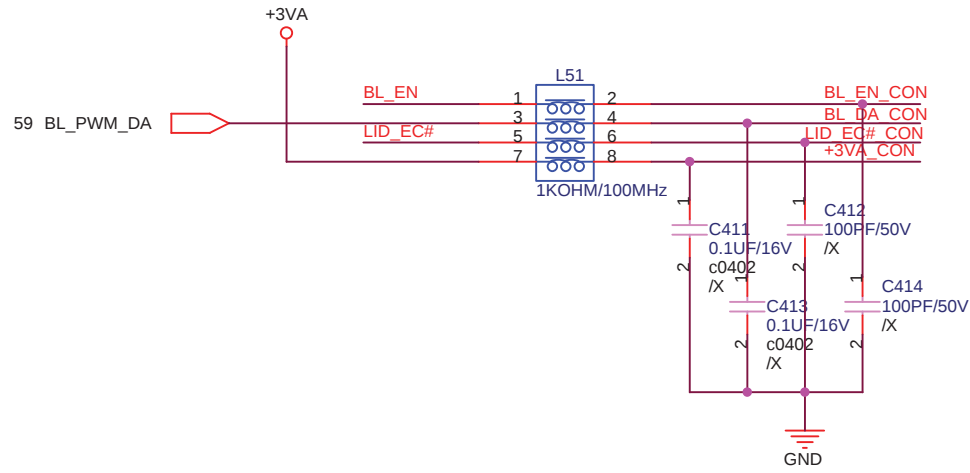
LCD LVDS Interface

LCD Power



INVERTER Interface/Speaker CONN.

BIOS
BACK_OFF#:When user push "Fn+F7"
button, BIOS active this pin to
turn off back light.

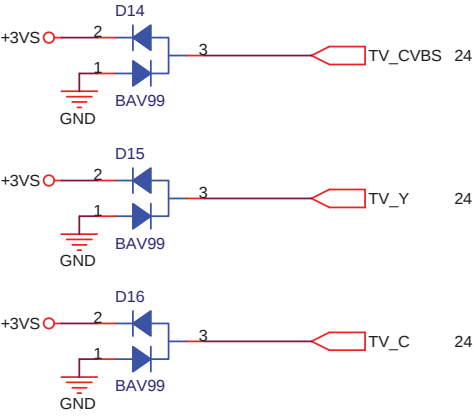


R1.01 remove HW reserve pannel ID

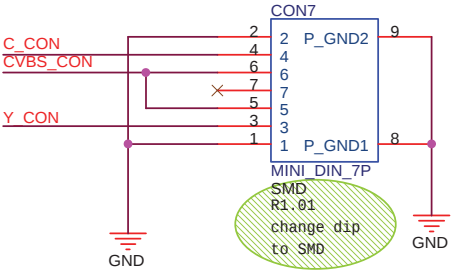
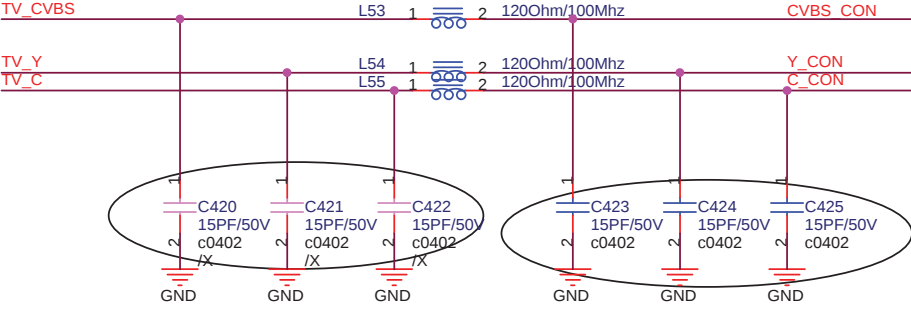
Title :LVDS & INVERTER
ASUSTeK COMPUTER INC
Engineer: **Alan Chu**

Size	Project Name	Rev
Custom	Z96J	1.0
Date: Wednesday, January 11, 2006		Sheet 33 of 92

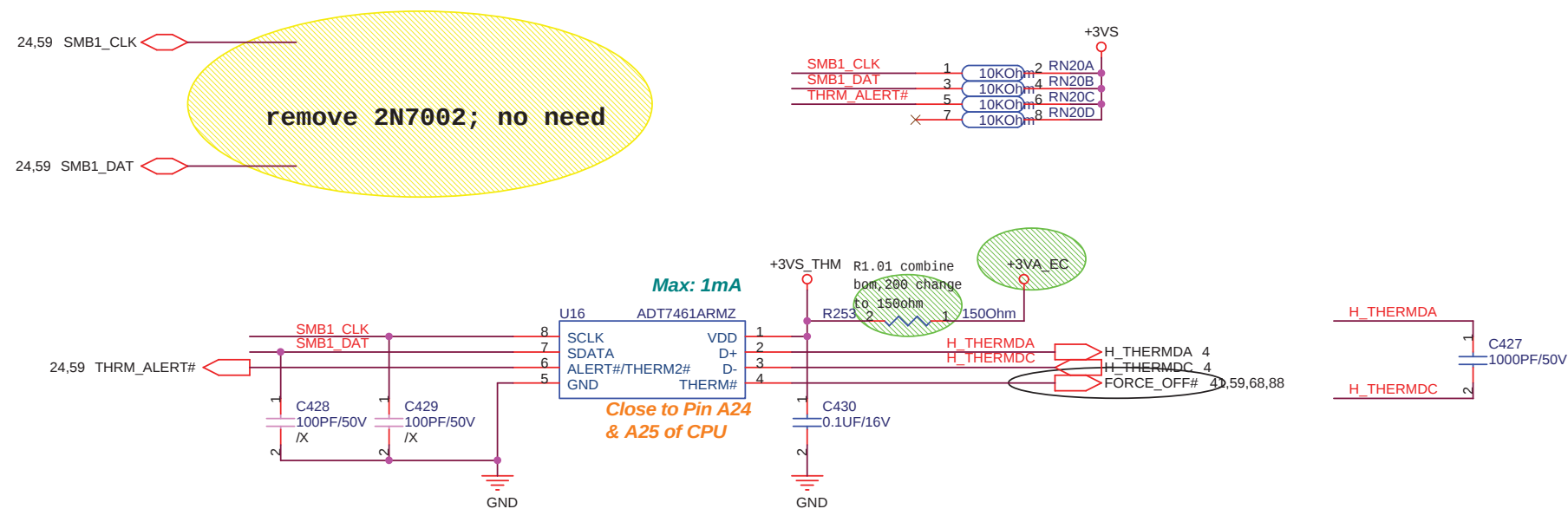
TV
OUT



PLACE ESD
Diodes near
TV port



Thermal Sensor



Route H_THERMDA and H_THERMDC on the same layer

-----OTHER SIGNALS

15 mils

=====GND

10 mils

=====H_THERMDA(10 mils)

10 mils

=====H_THERMDC(10 mils)

10 mils

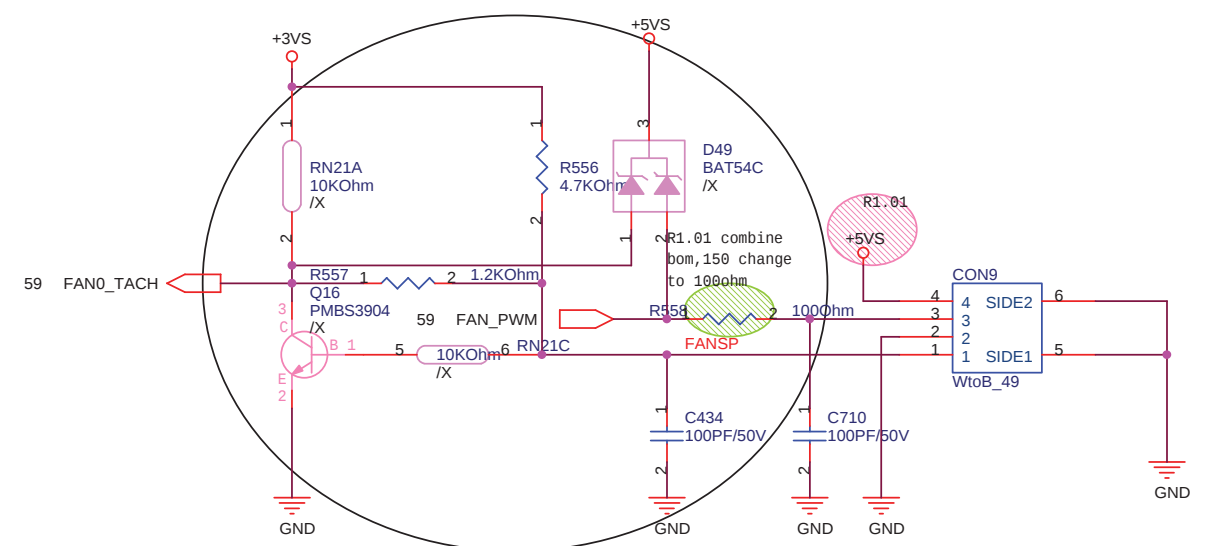
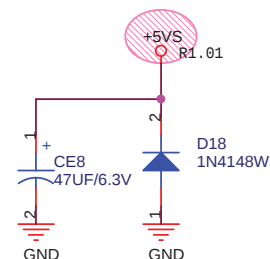
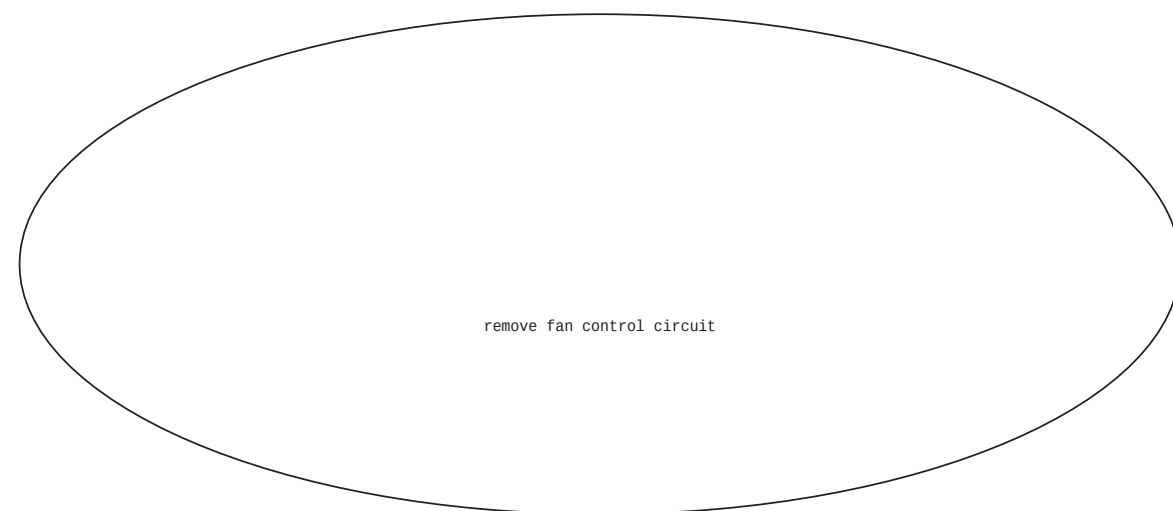
=====GND

15 mils

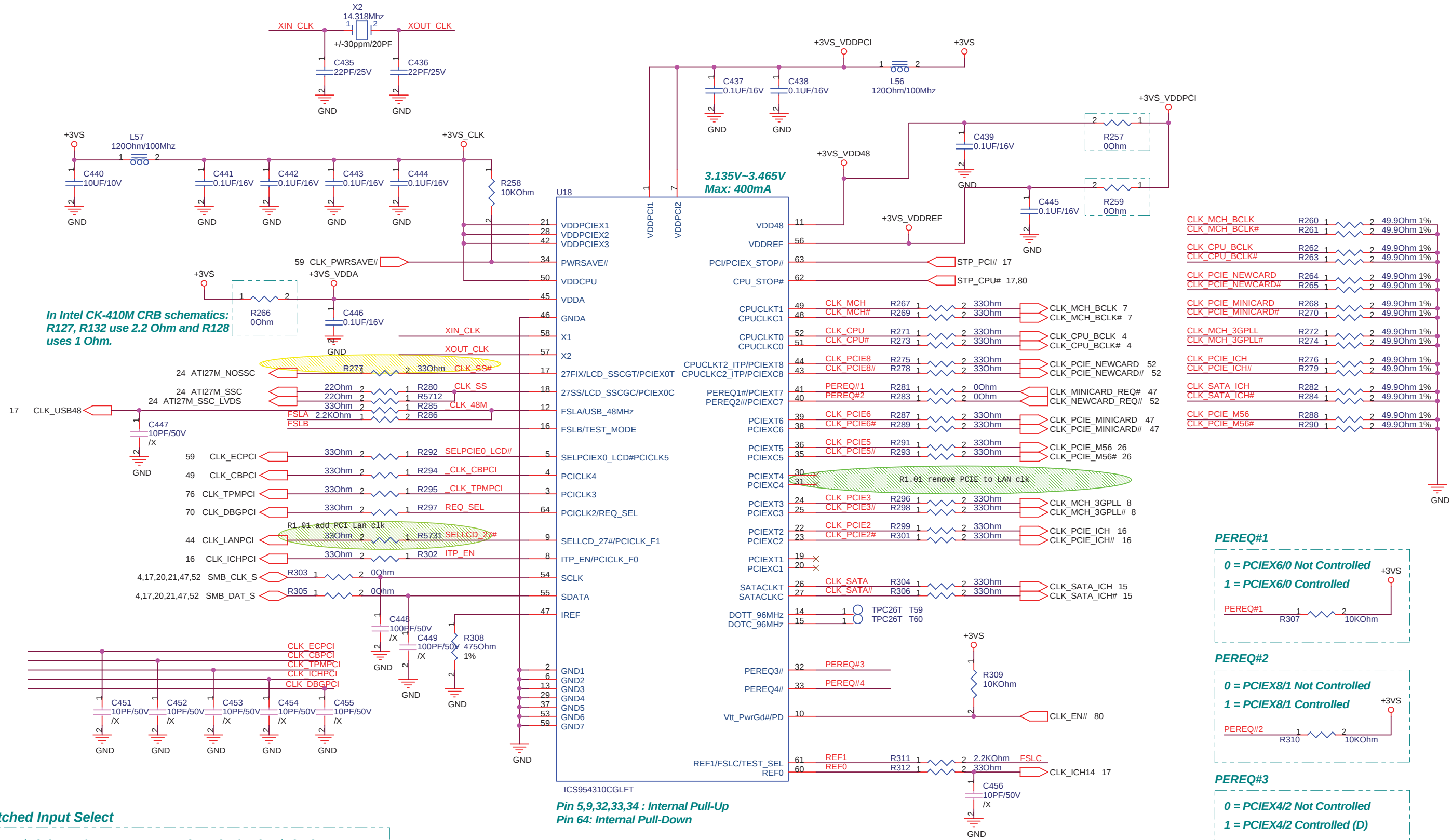
-----OTHER SIGNALS

Avoid FSB,Power

DC FAN Control



CPU FAN will be forced on:
 1) Thermal Sensor Over-temperature
 2) WATCHDOG asserted by EC



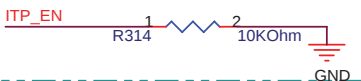
In Intel CK-410M CRB schematics:
R127, R132 use 2.2 Ohm and R128
uses 1 Ohm.

Pin 5,9,32,33,34 : Internal Pull-Up
Pin 64: Internal Pull-Down

Latched Input Select

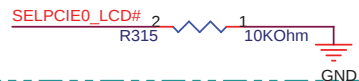
ITP_EN/PCICLK_F0

0 = SRC Pair
1 = CPU_I/P Pair



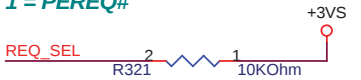
SELPCIE0_LCD#/PCI_CLK5

0 = LCD Clock (96MHz)
1 = PCI Express (100MHz)



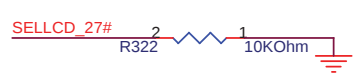
PCI_CLK2/REQ_SEL

0 = PCICLK(D)
1 = PEREQ#

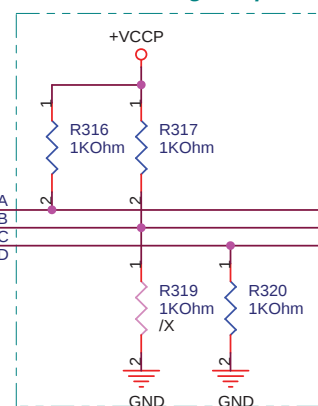


SELLCD_27#/PCICLK_F1

0 = 27MHzSS/27MHzSS# Pair
1 = LCD_CLK Pair



Reserved for Debug & Exprimt



BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

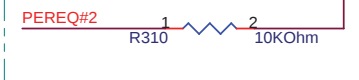
PEREQ#1

0 = PCIE6/0 Not Controlled
1 = PCIE6/0 Controlled



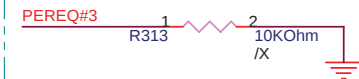
PEREQ#2

0 = PCIE8/1 Not Controlled
1 = PCIE8/1 Controlled



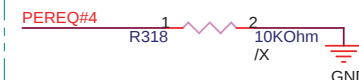
PEREQ#3

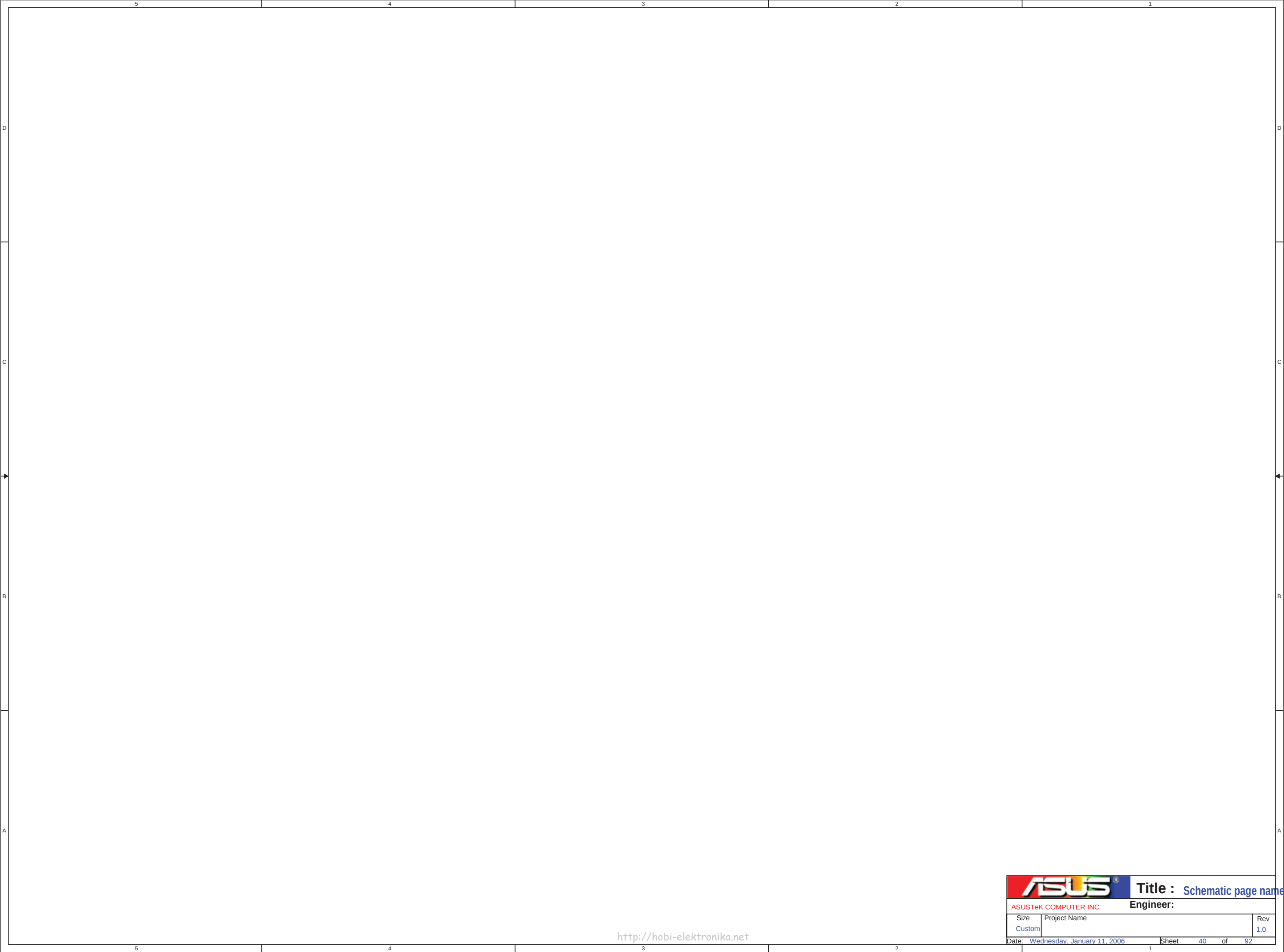
0 = PCIE4/2 Not Controlled
1 = PCIE4/2 Controlled (D)



PEREQ#4

0 = PCIE7/5/3 Not Controlled
1 = PCIE7/5/3 Controlled (D)







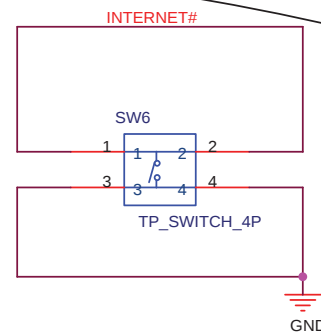
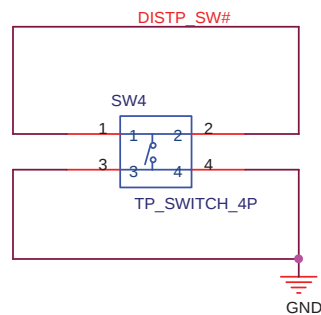
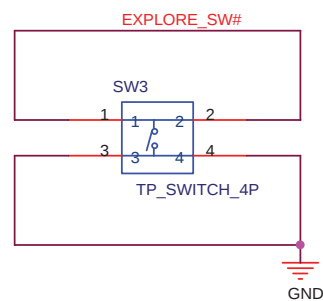
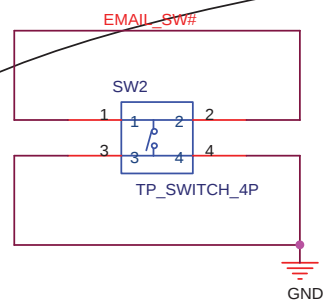
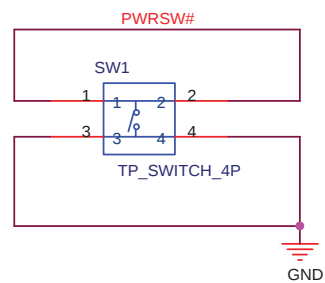
Title : Schematic page name

ASUSTeK COMPUTER INC

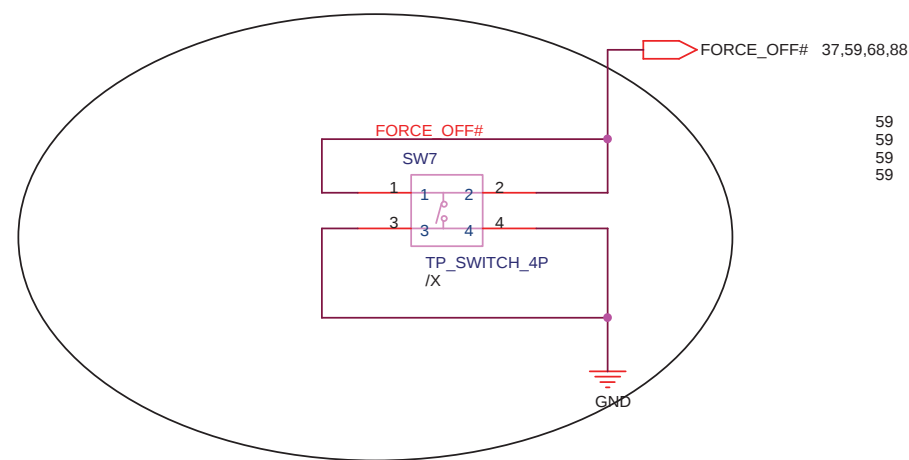
Engineer:

Size	Project Name	Rev
Custom		1.0

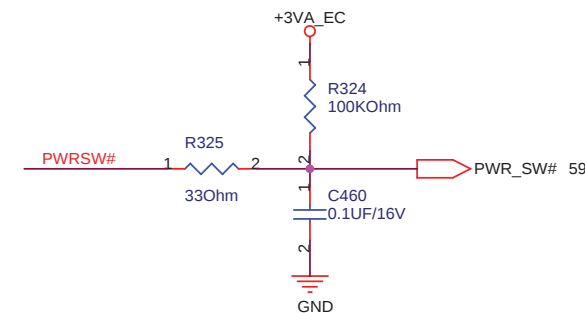
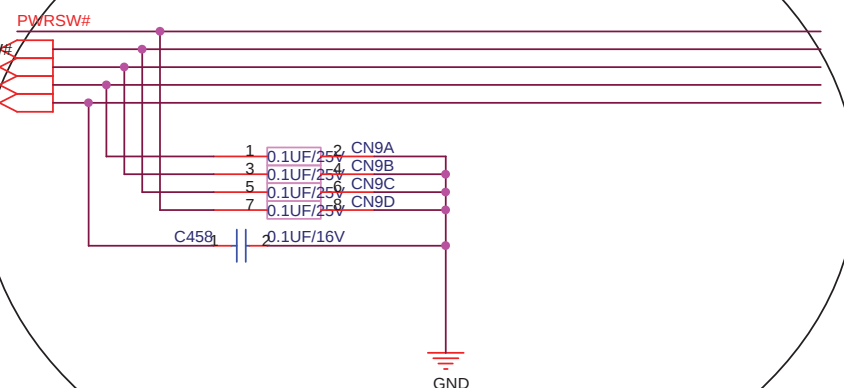
Date: Wednesday, January 11, 2006Sheet 40 of 92



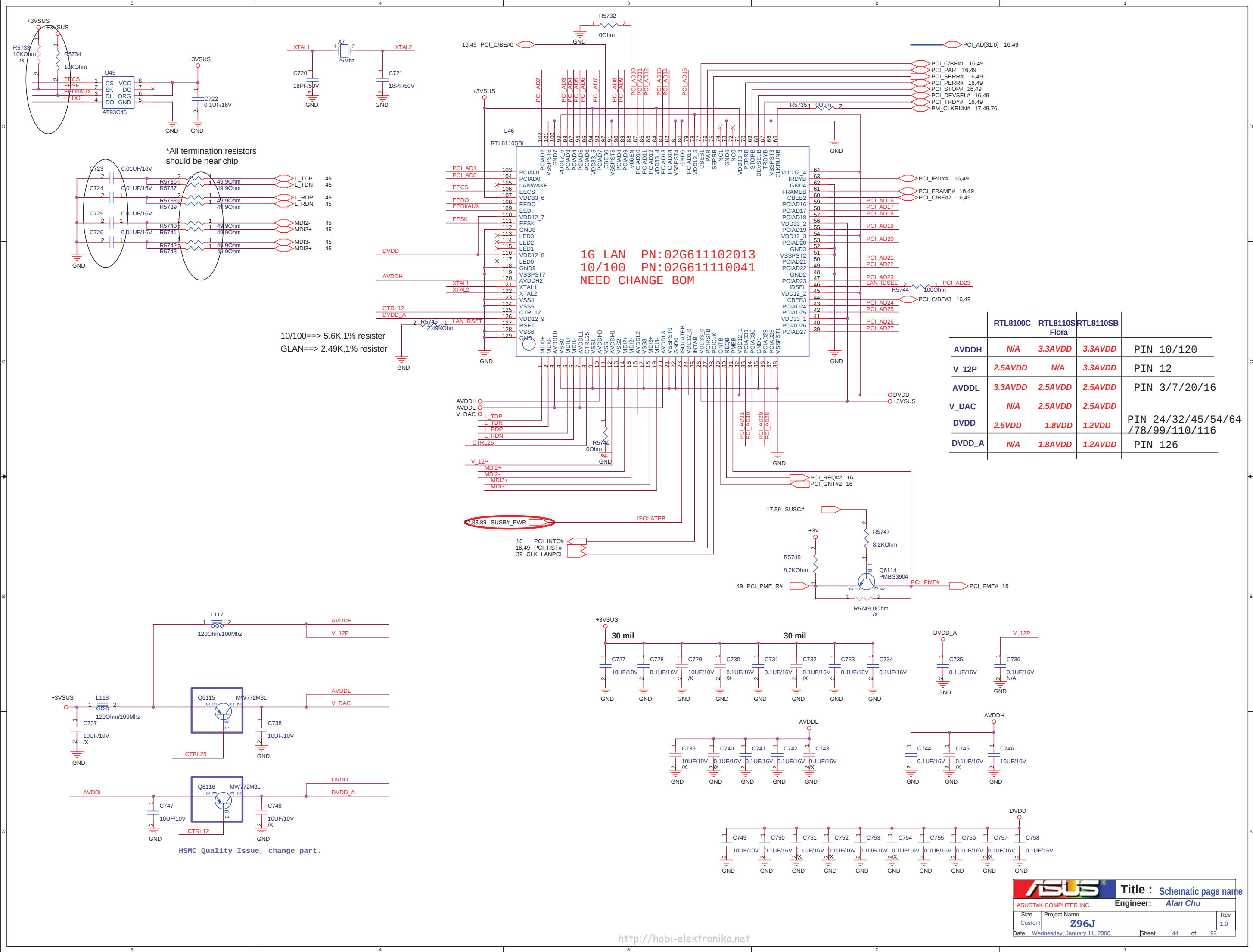
SHUT_DOWN#



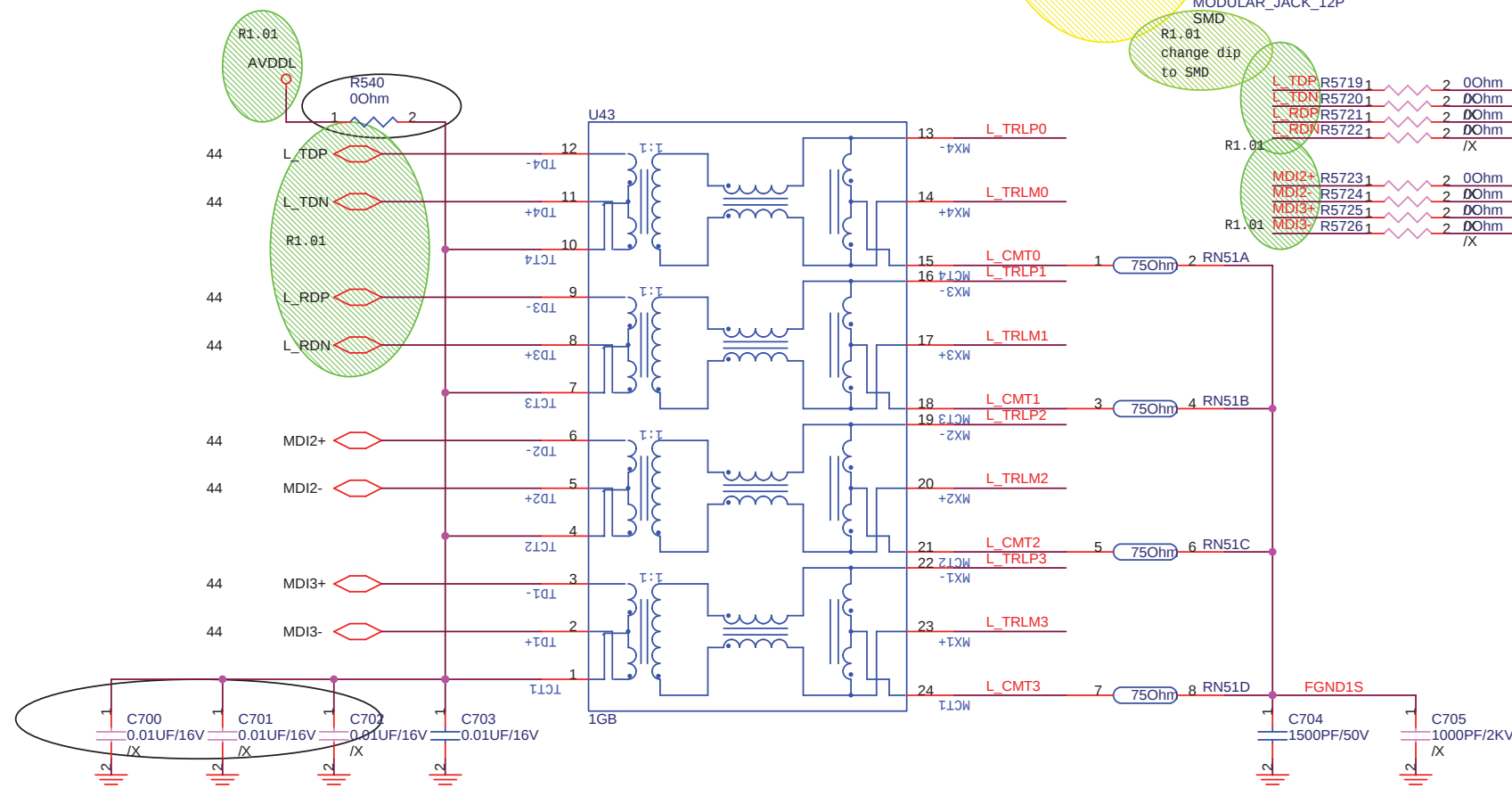
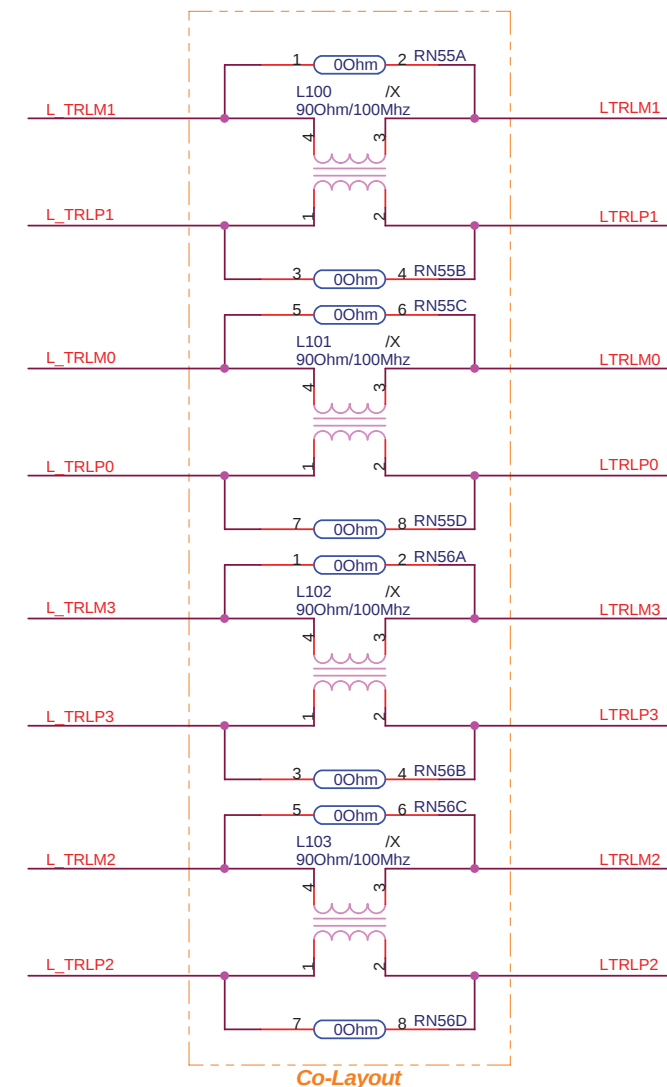
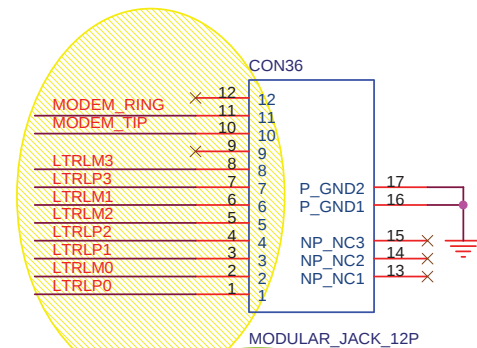
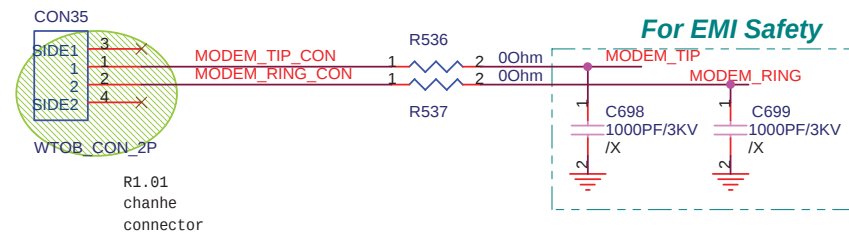
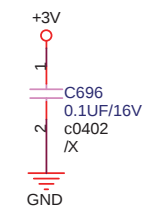
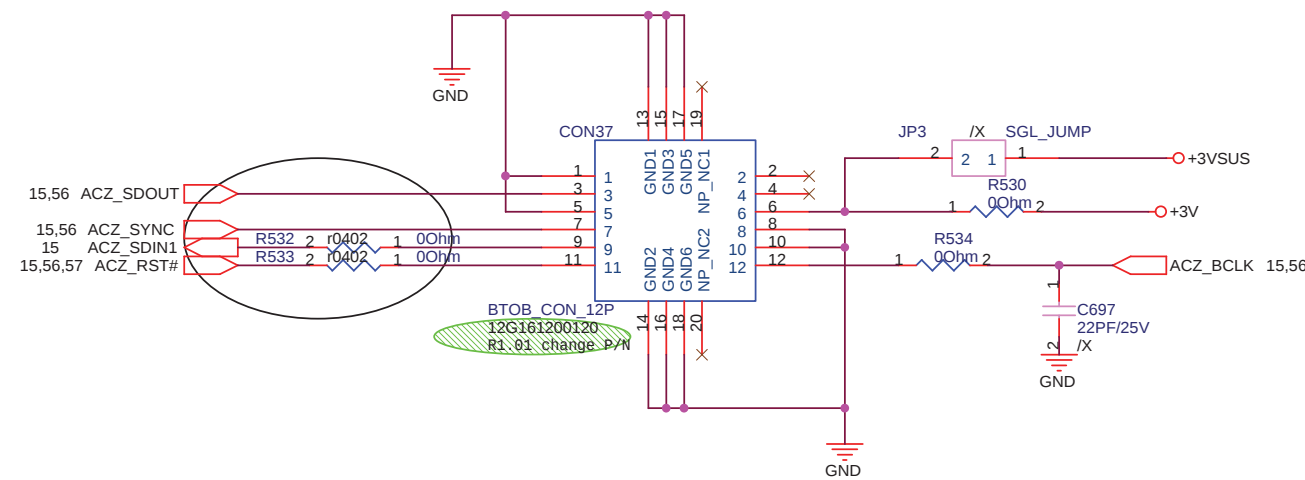
59 EXPLORE_SW#
59 DISTP_SW#
59 INTERNET#
59 EMAIL_SW#

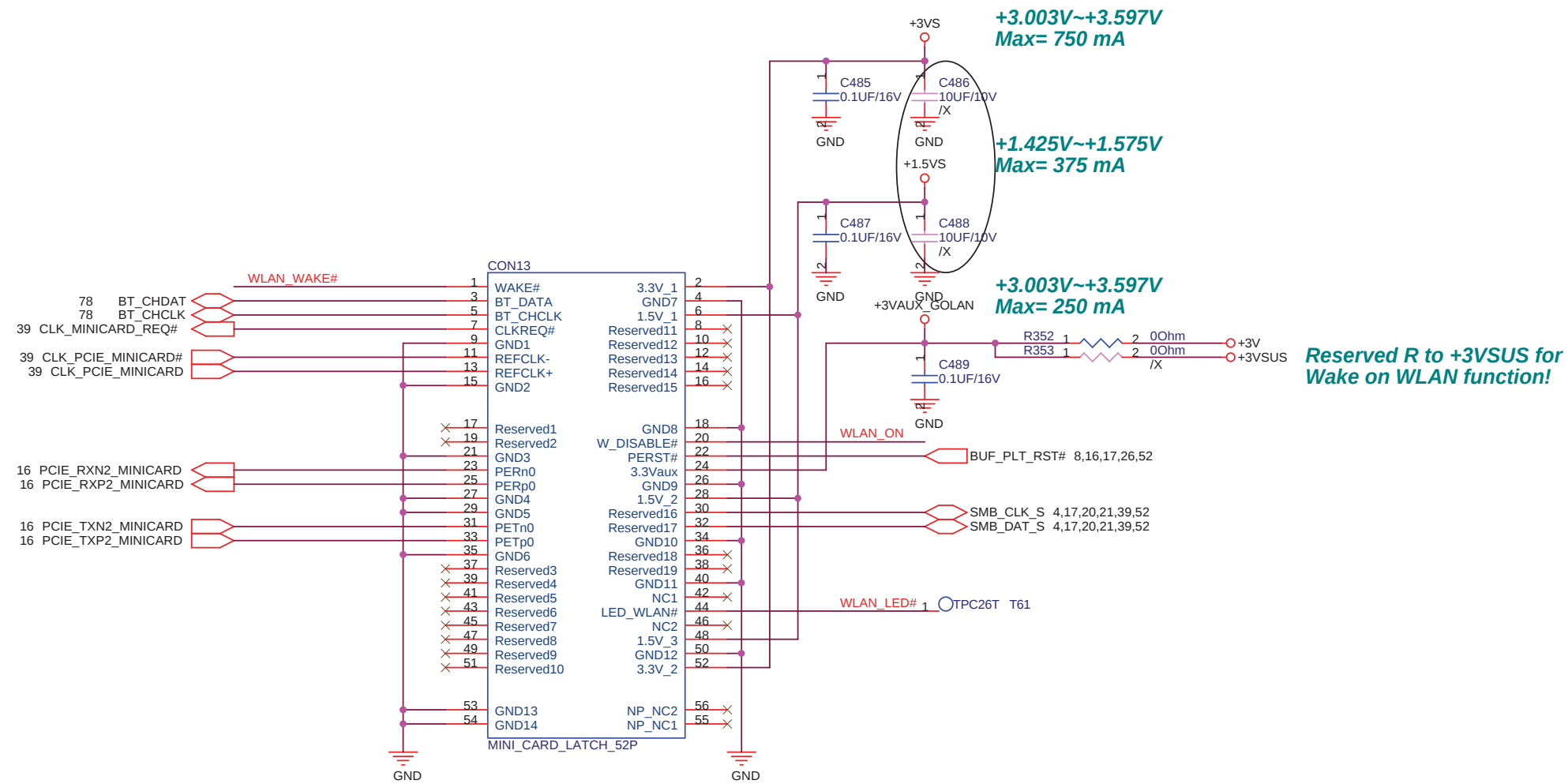






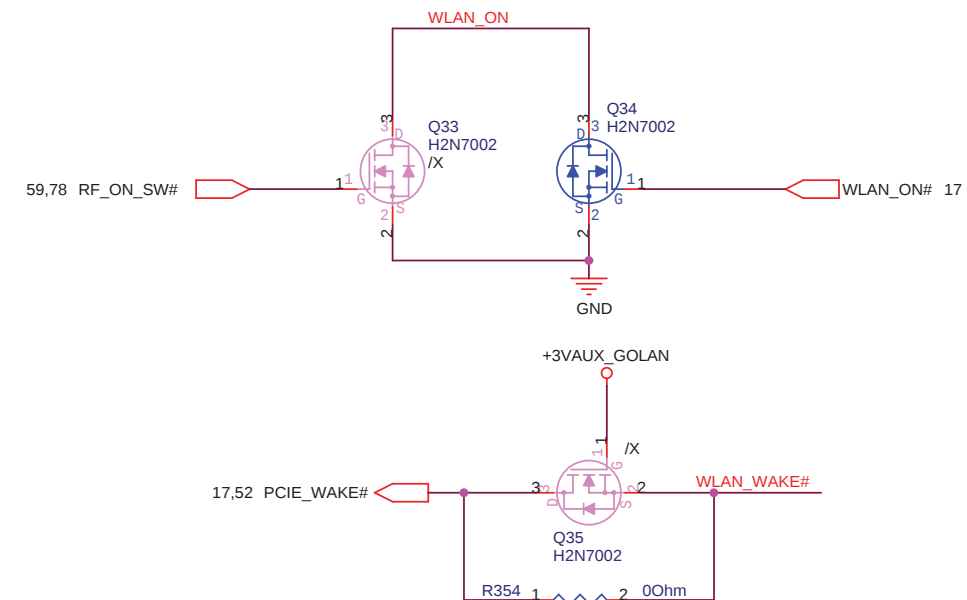
MDC CONN.

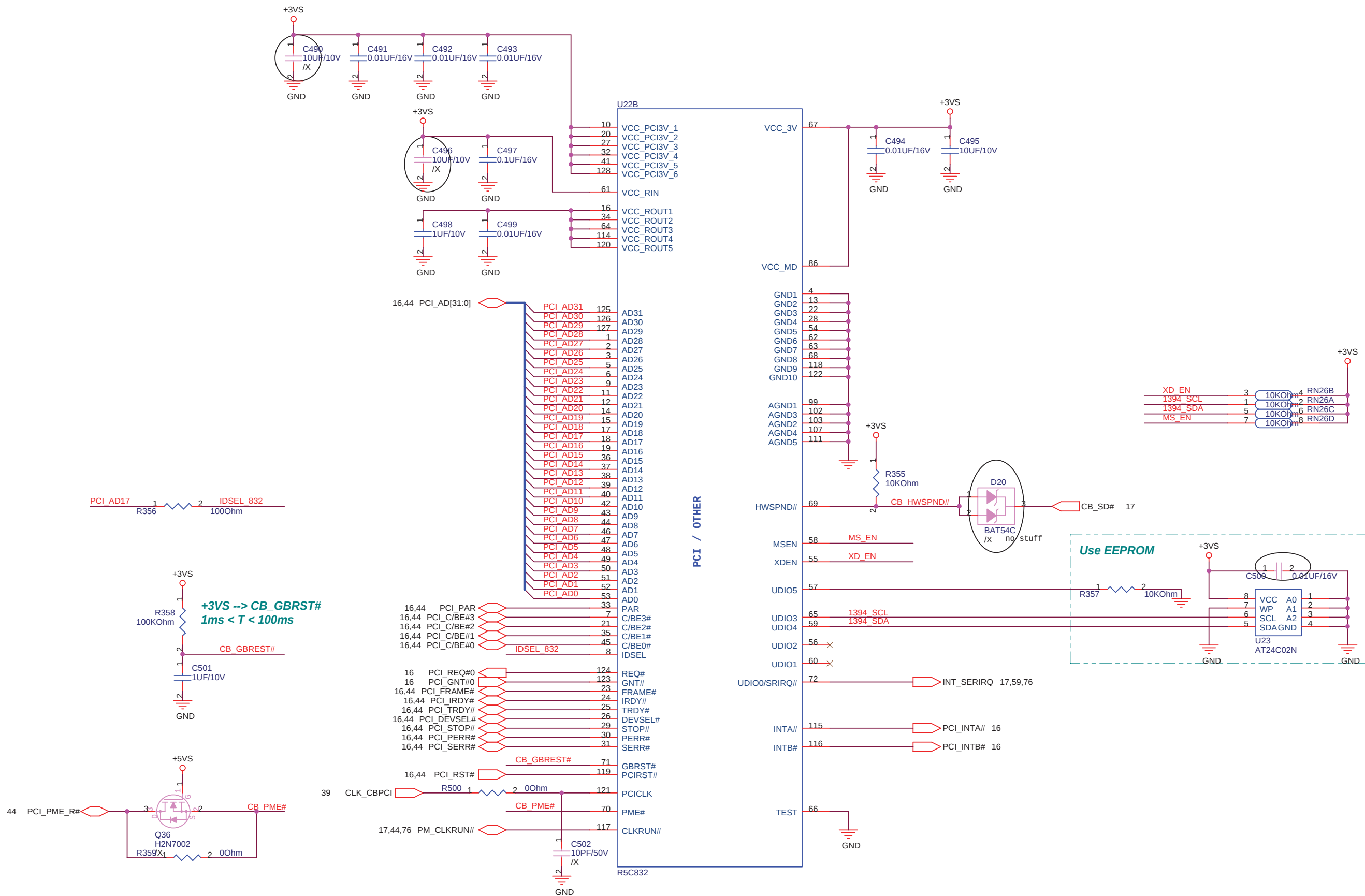




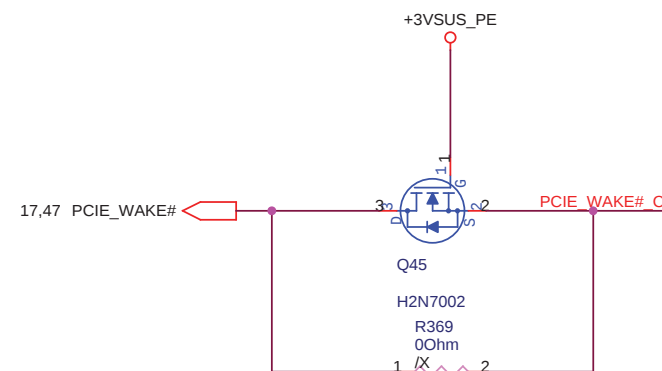
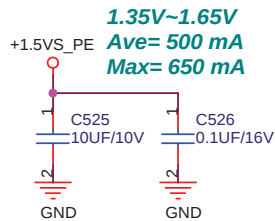
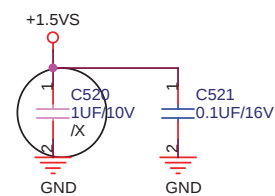
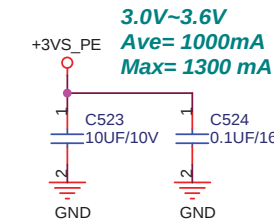
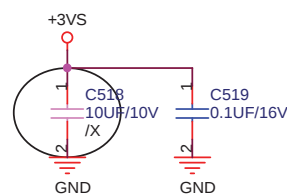
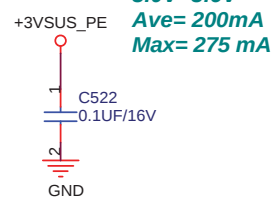
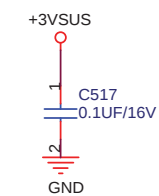
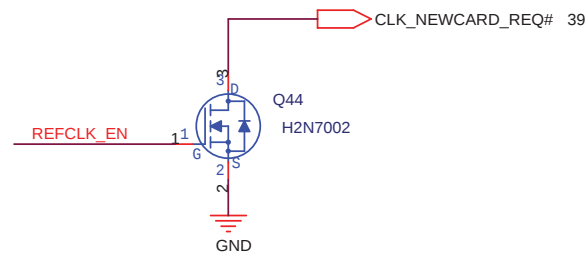
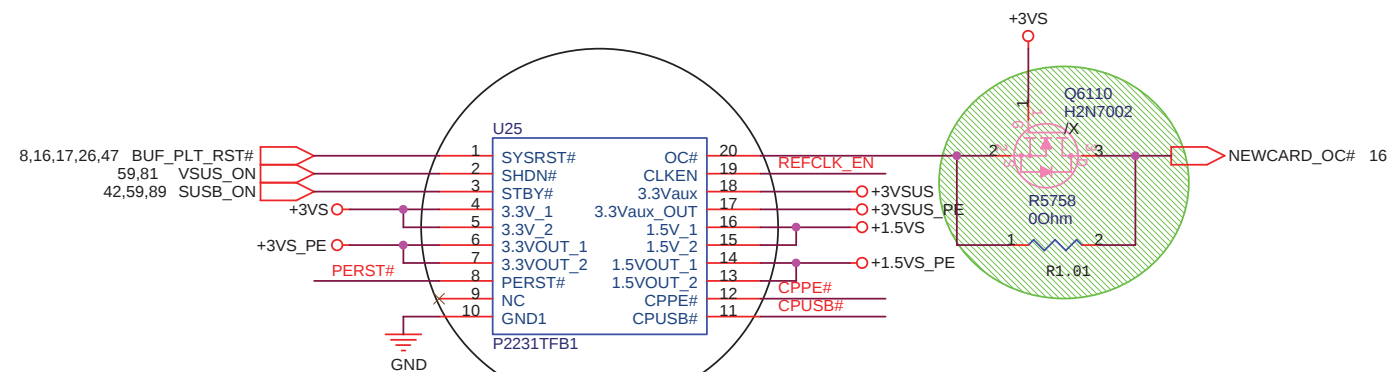
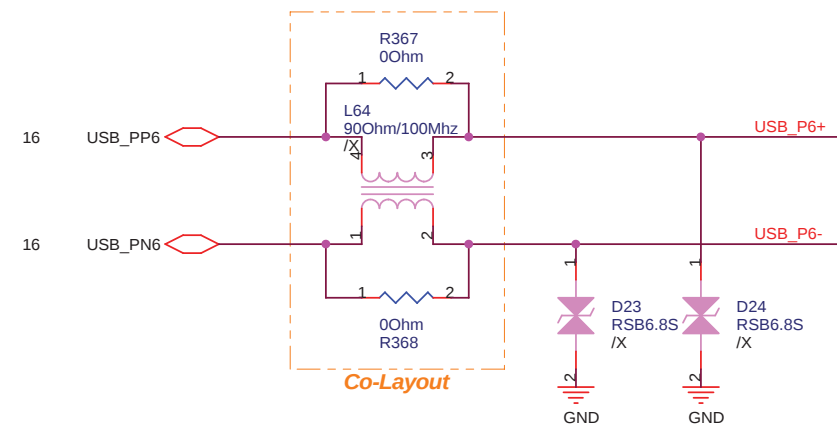
H54 & H56

R1.01 remove connector, change to screw

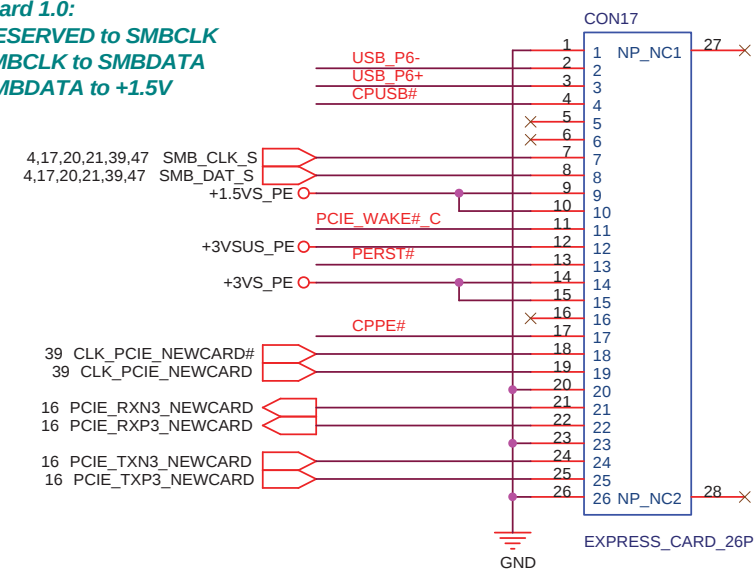






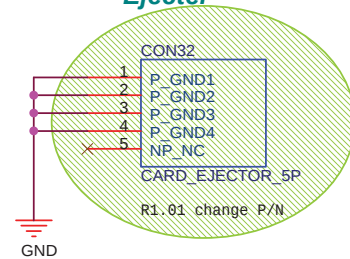


!! ExpressCard Standard 1.0:
 Change Pin7 from RESERVED to SMBCLK
 Change Pin8 from SMBCLK to SMBDATA
 Change Pin9 from SMBDATA to +1.5V

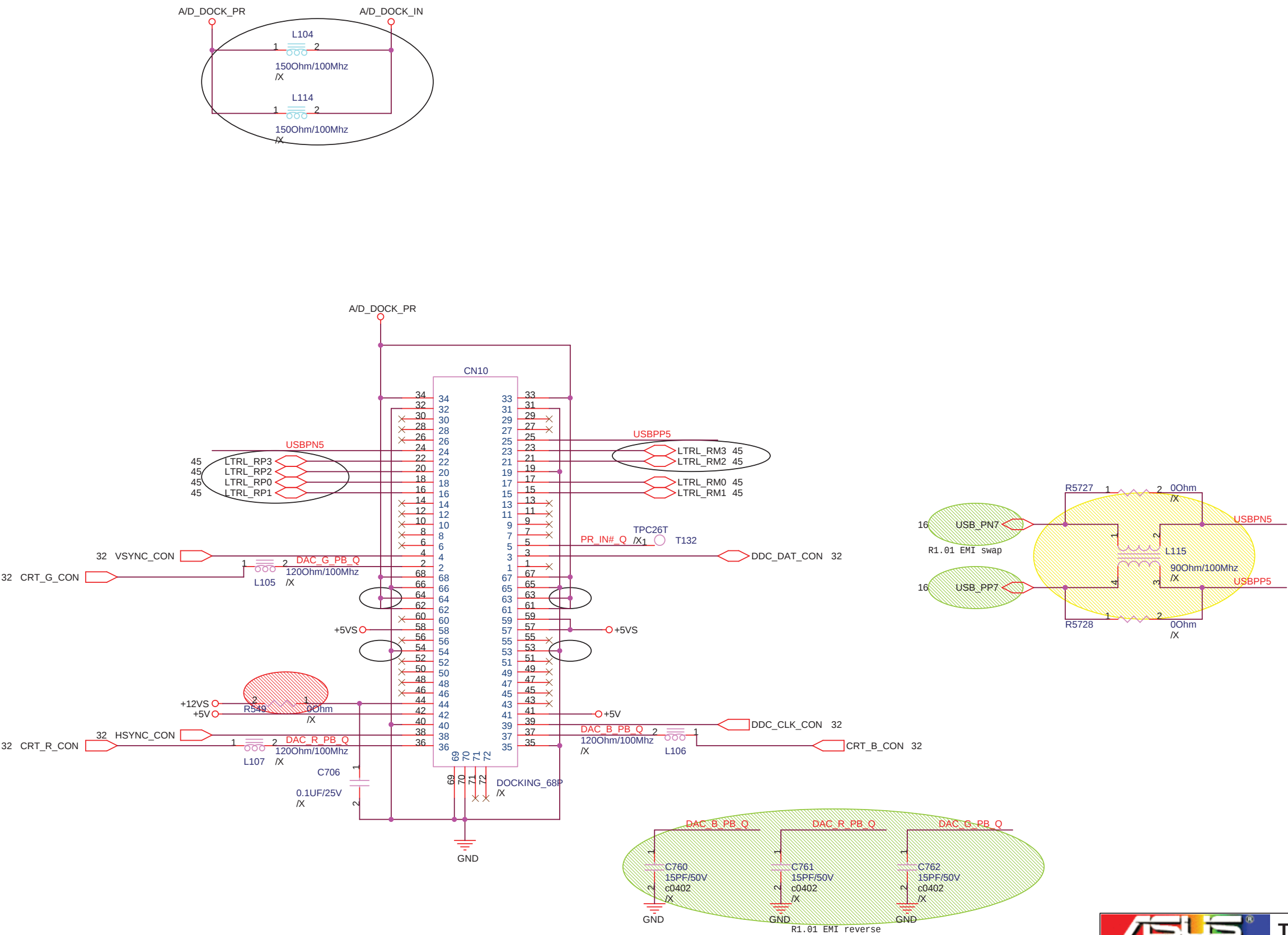


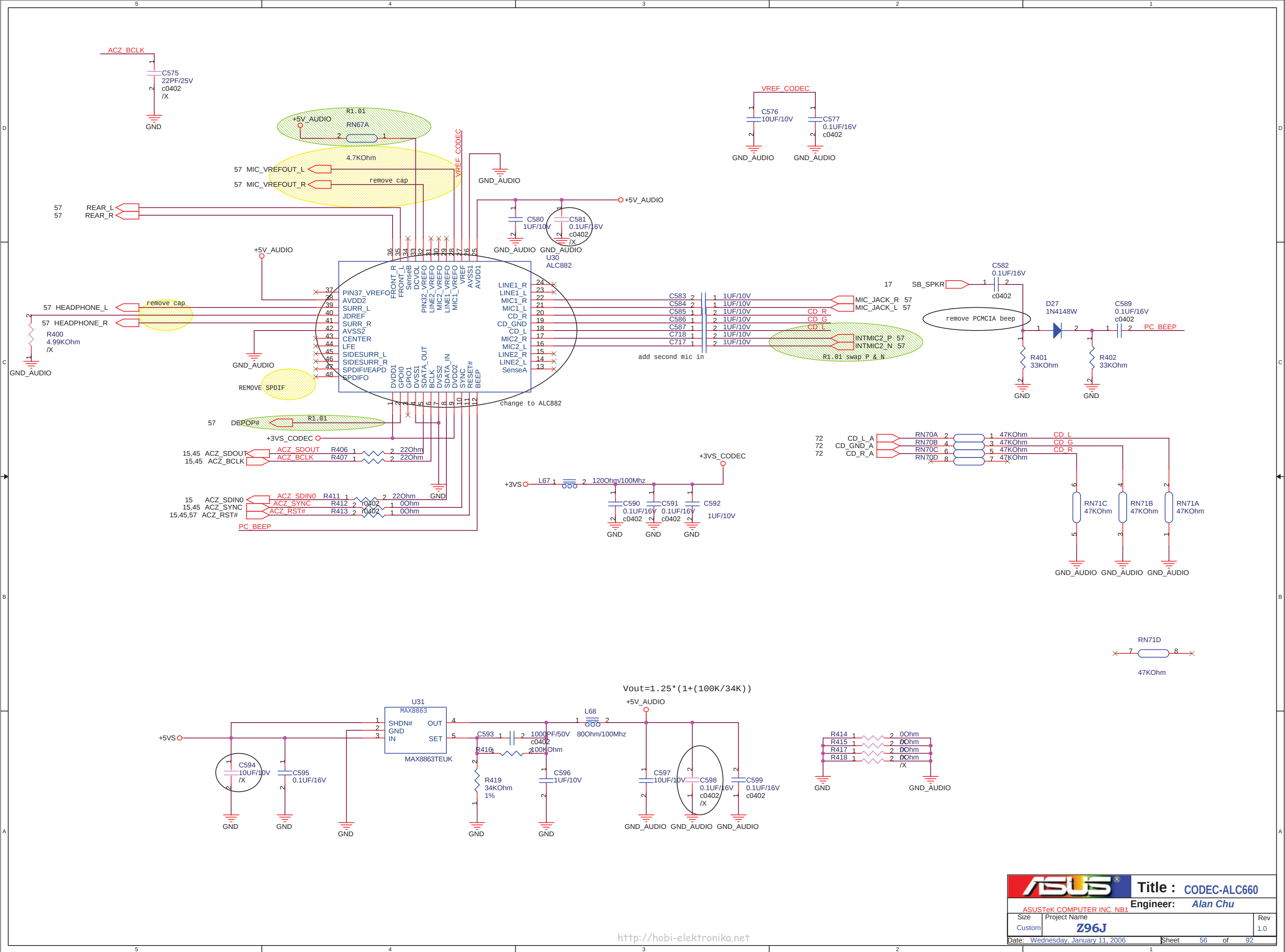
NewCard Header

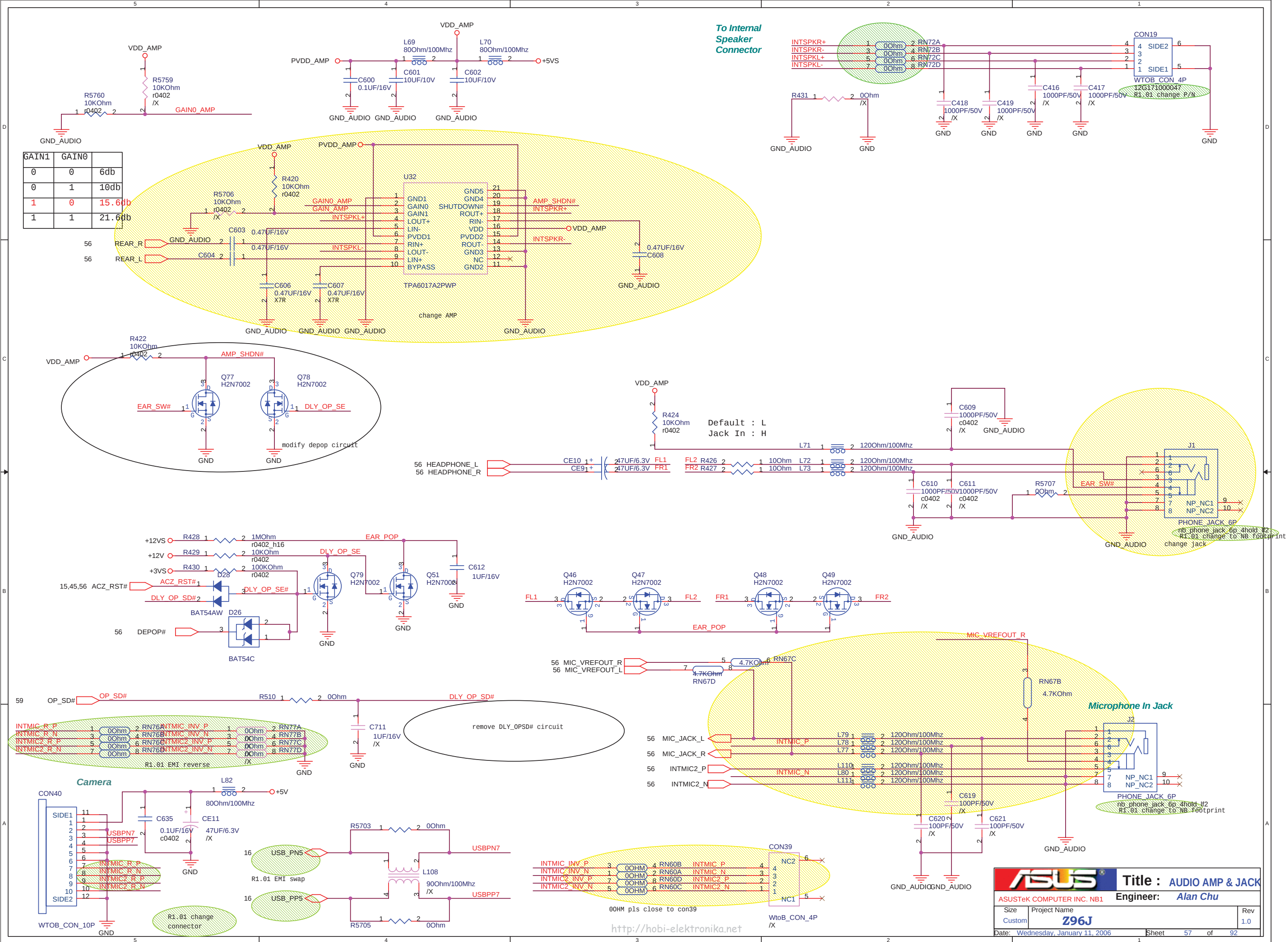
NewCard Ejecter



PORT BAR III

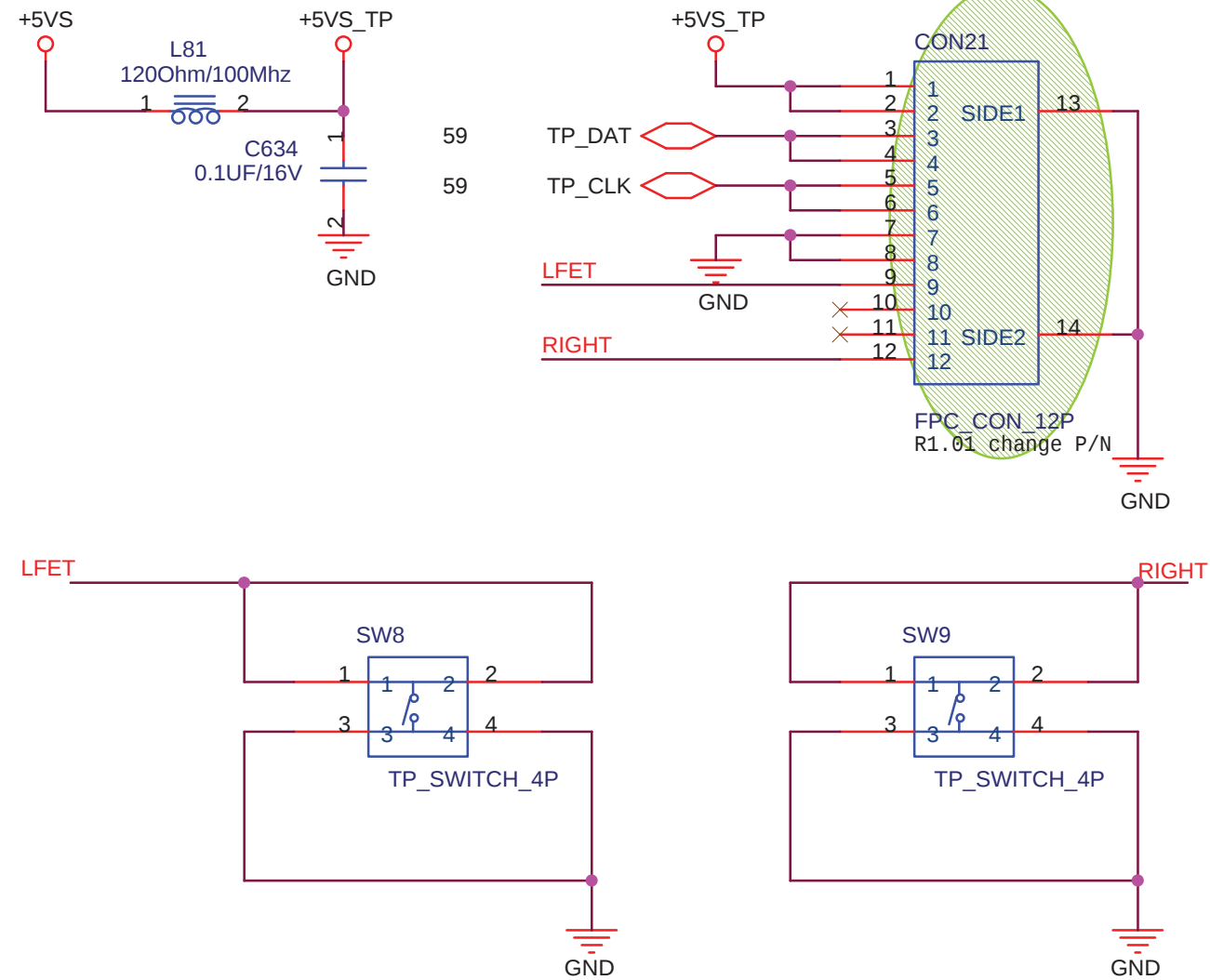




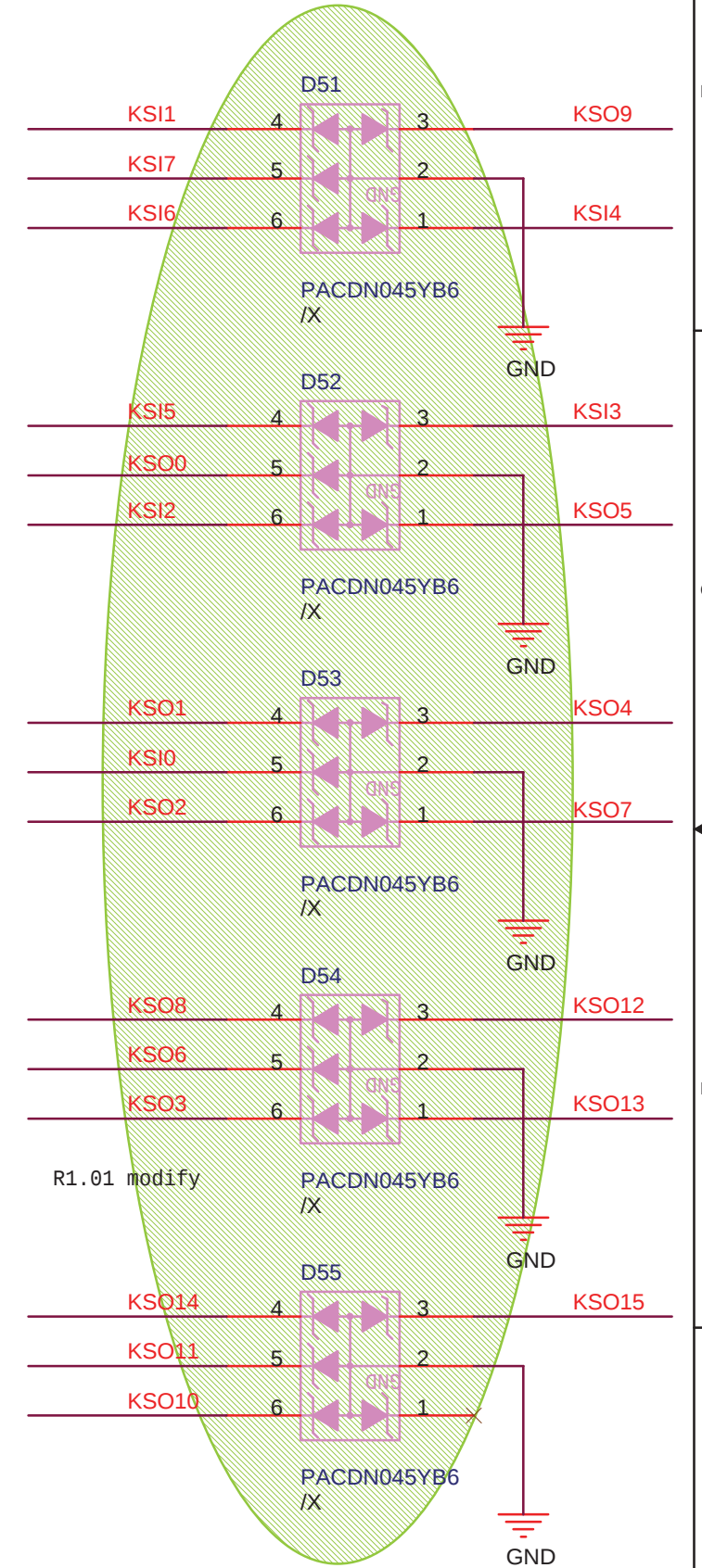
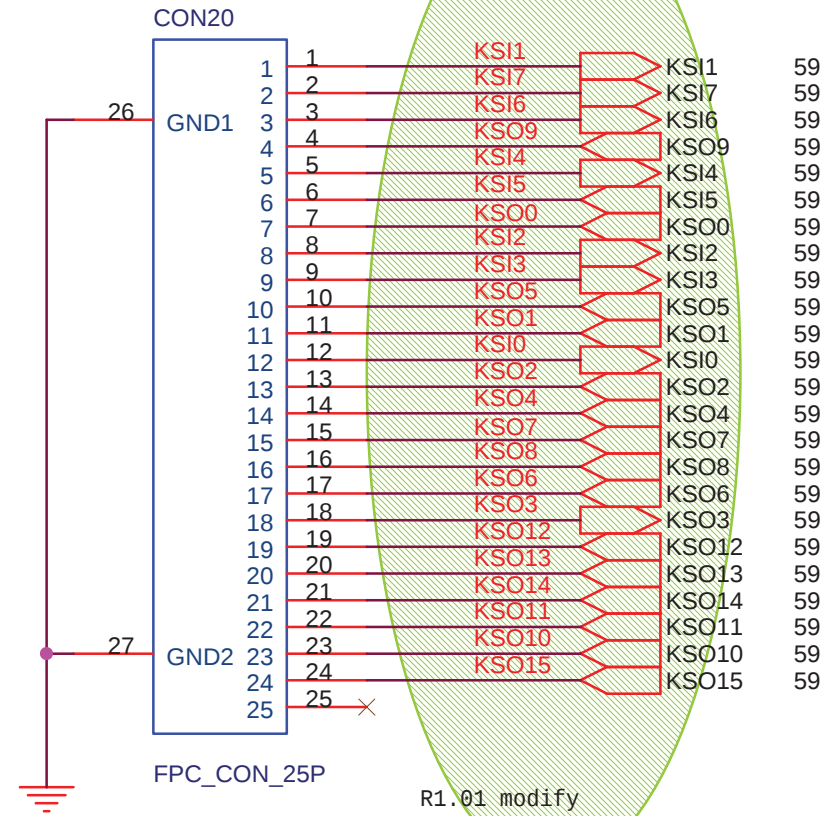




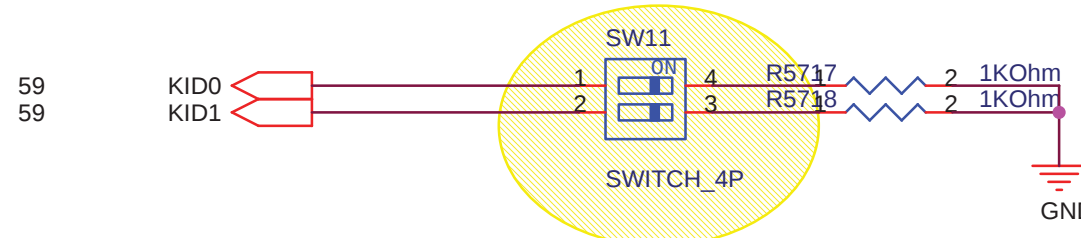
For Touch-Pad

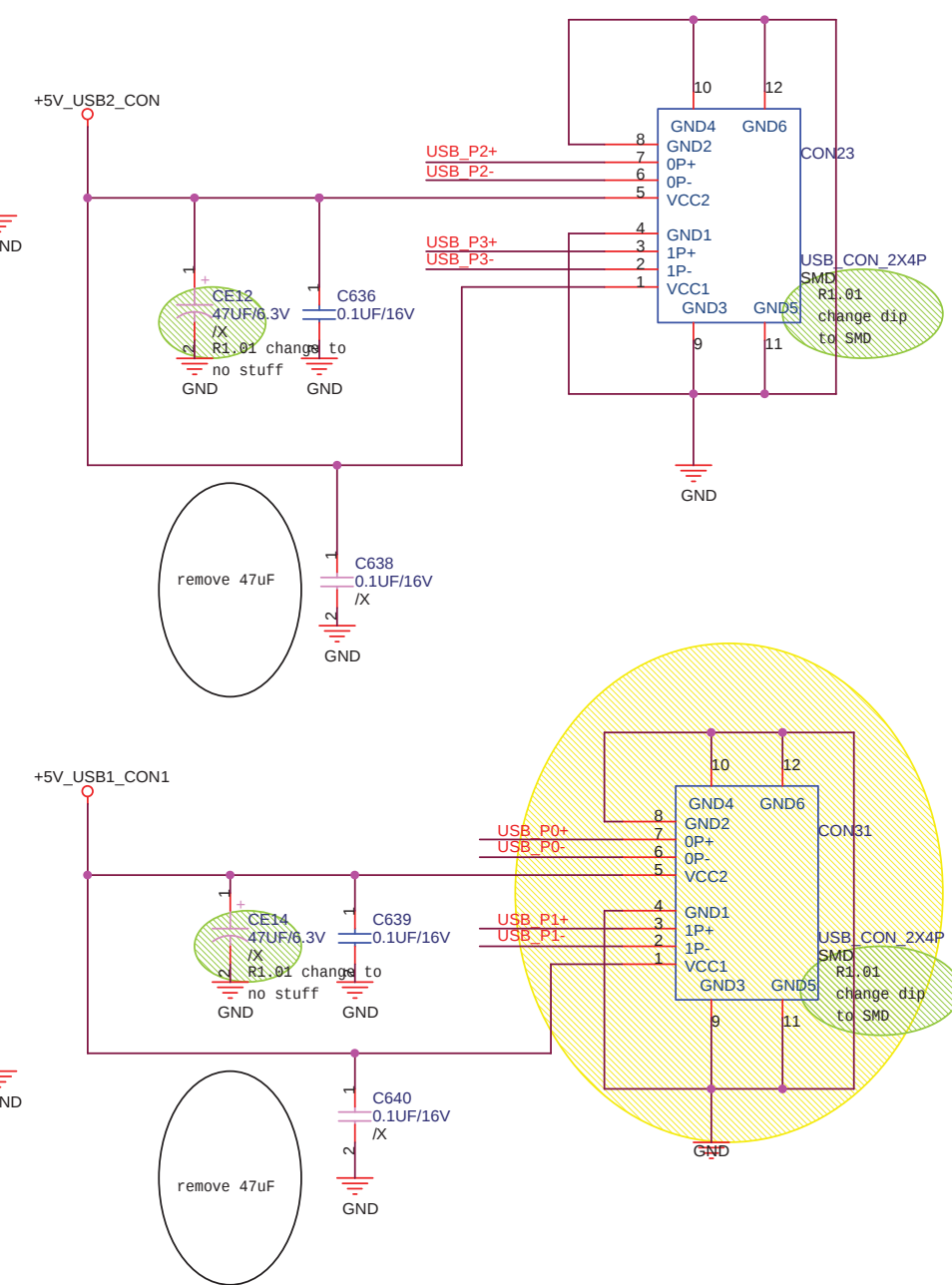
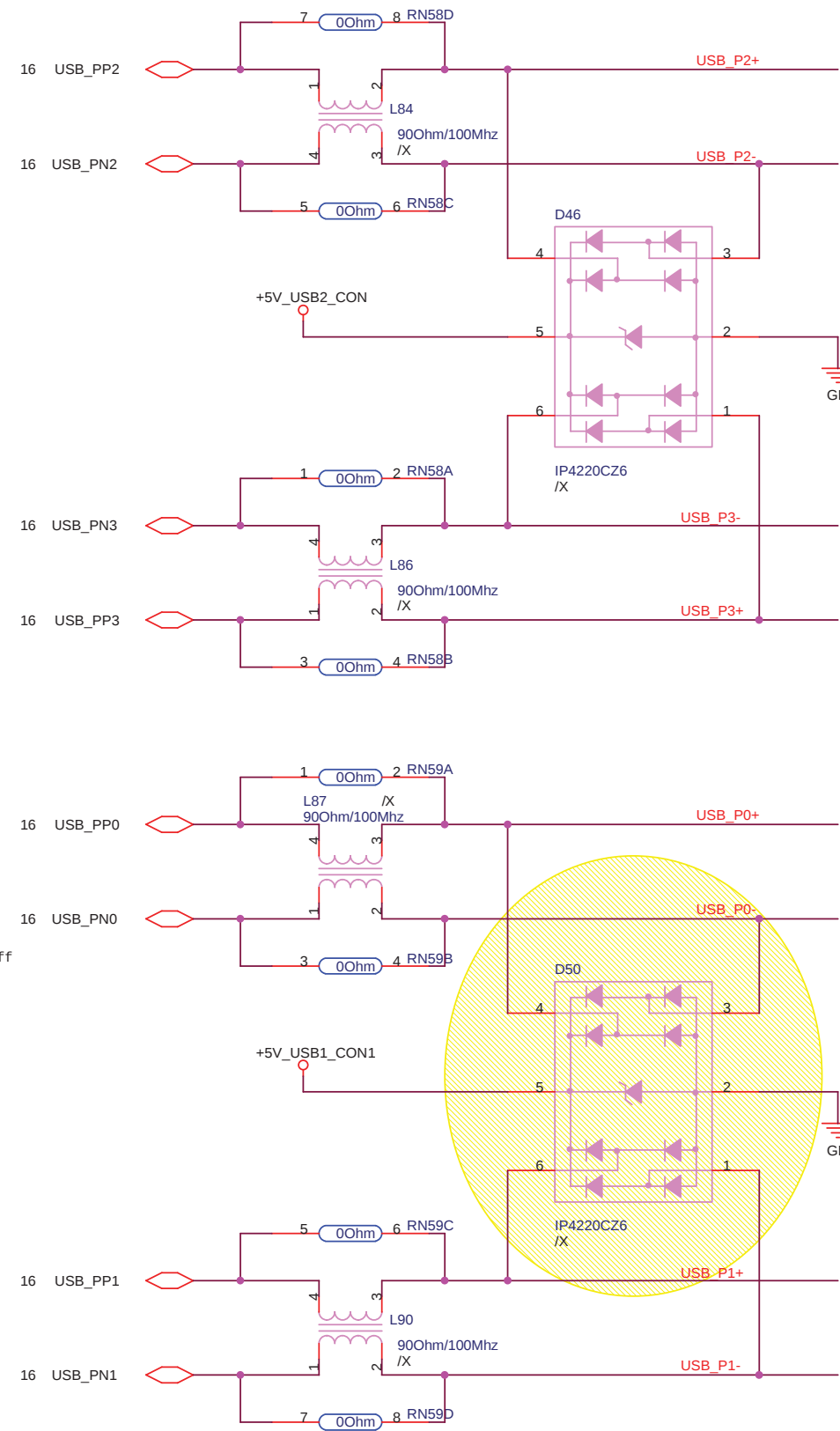
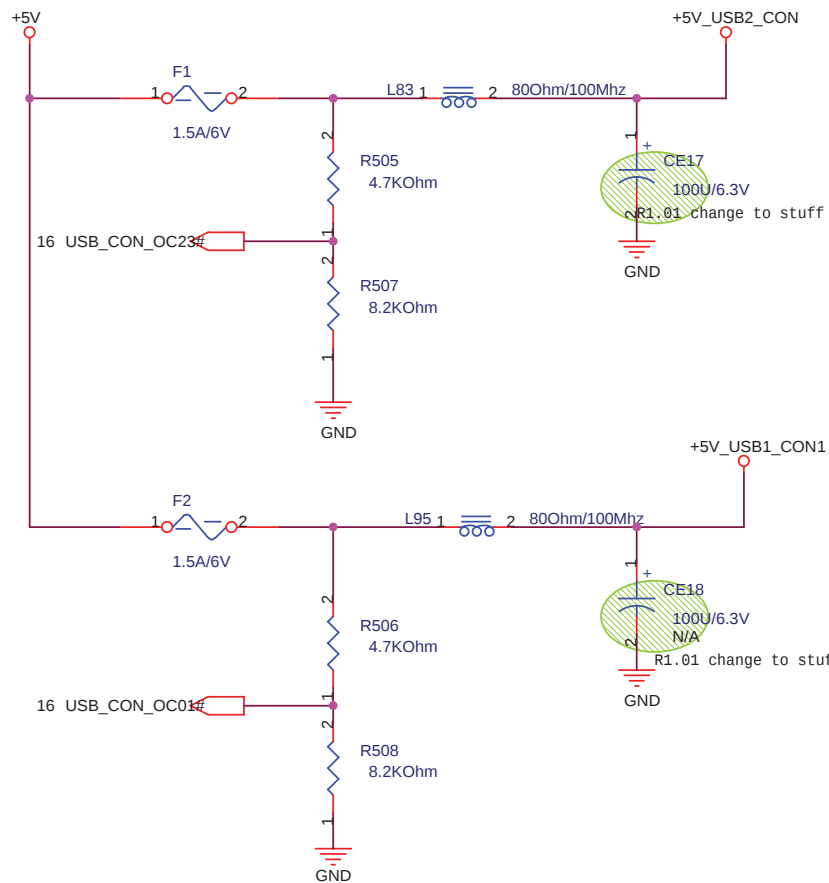


For Keyboard



remove pull high, already pull high



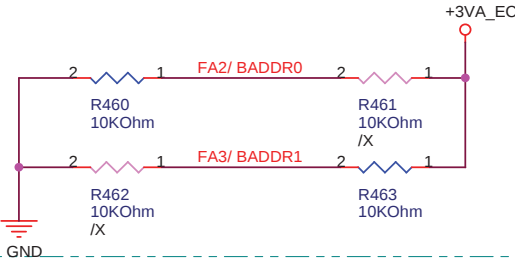


ISA ROM

EC Hardware Strapping

FA2/ BADDR0 & FA3/ BADDR1

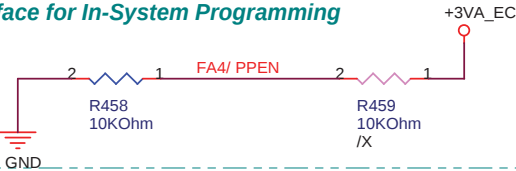
00: PNPCNG Access Register Pair Are 002Eh and 002Fh
10: PNPCNG Access Register Pair Are 004Eh and 004Fh
01: PNPCNG Access Register Pair Are Determined by
EC Domain Registers SWCBALR and SWCBAHR.
11: Reserved



Note: Sampled at VSTBY Power Up Reset

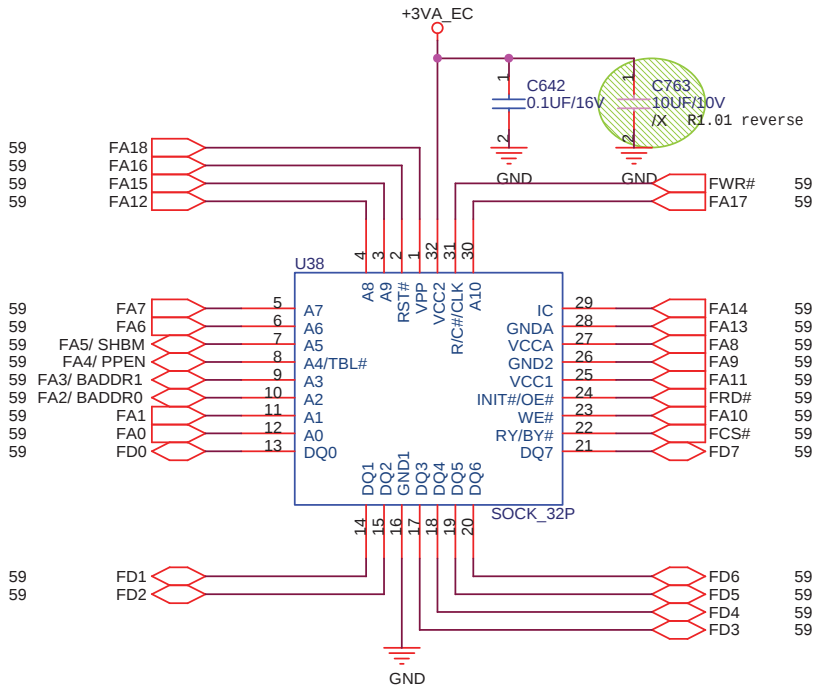
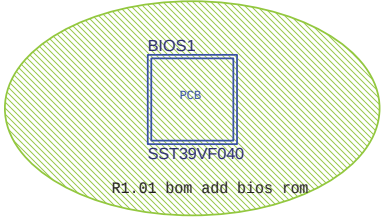
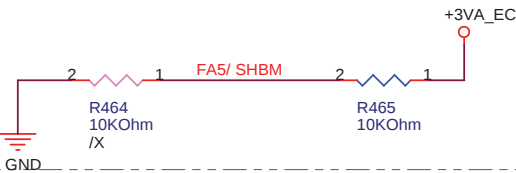
FA4/ PPEN

0: Normal
1: KBS Interface Pins Are Switched to Parallel Port
Interface for In-System Programming



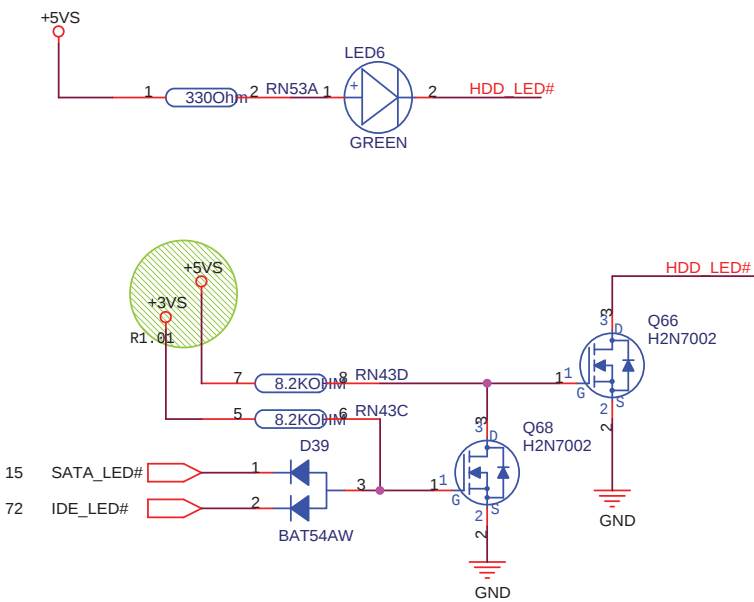
FA5/ SHBM

0: Disable Shared Memory with Host BIOS
1: Enable Shared Memory with Host BIOS

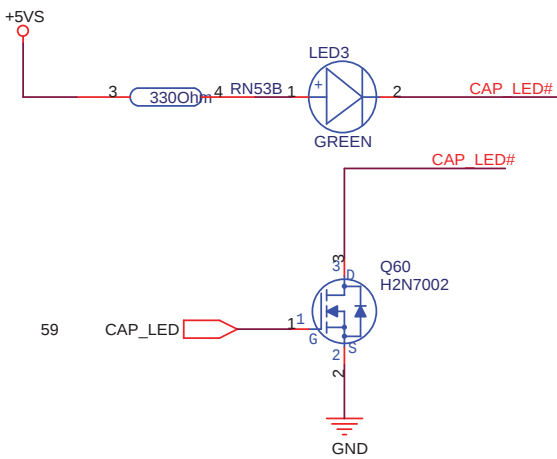


For LED

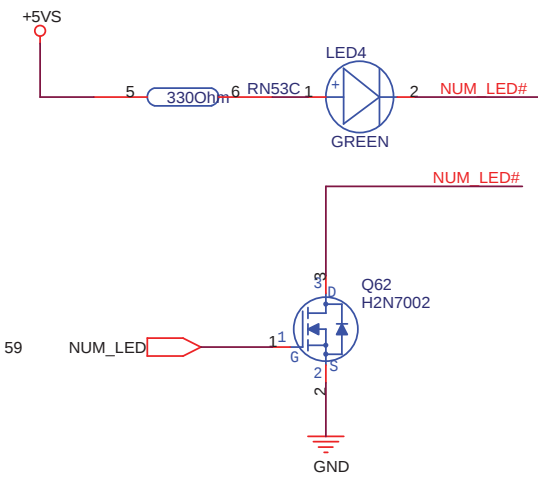
For SATA/IDE LED



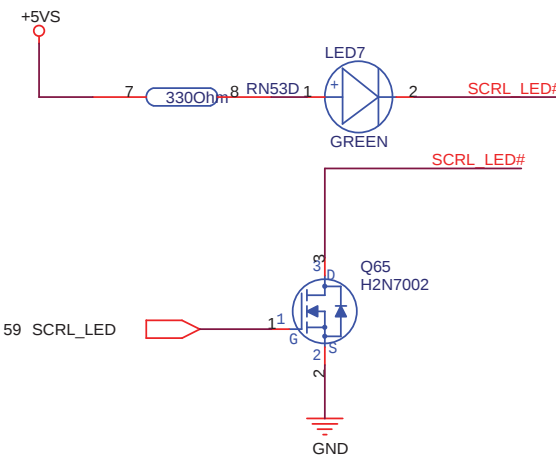
for Cap. Lock



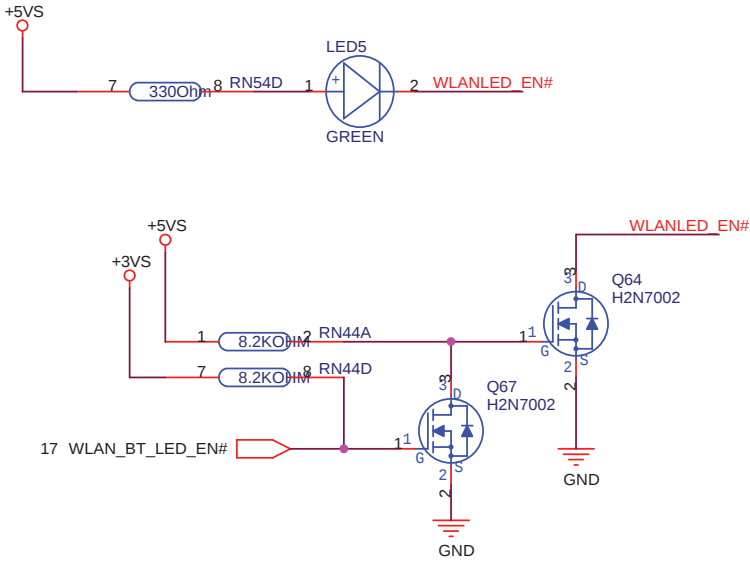
for Num Lock



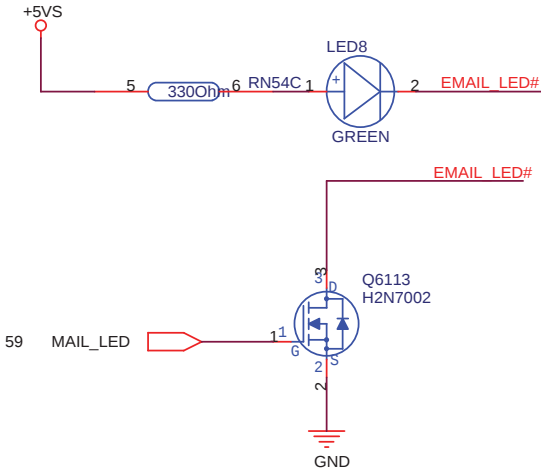
for Scroll Lock



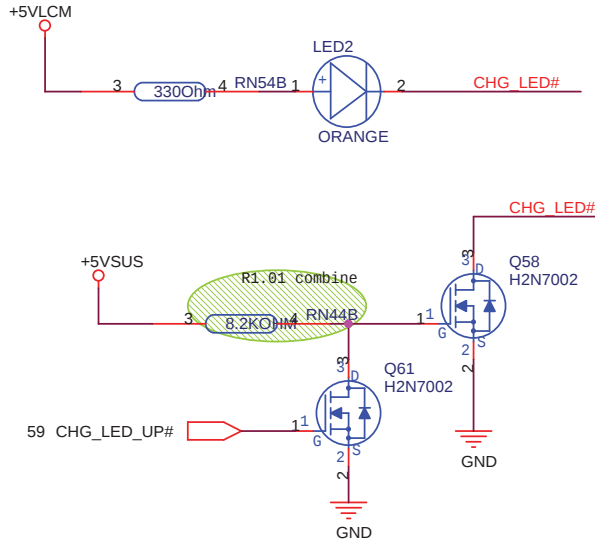
For WireLess LED



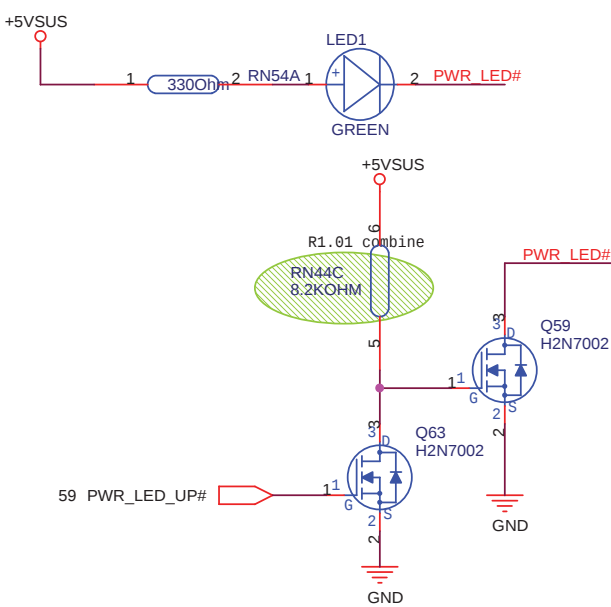
for email



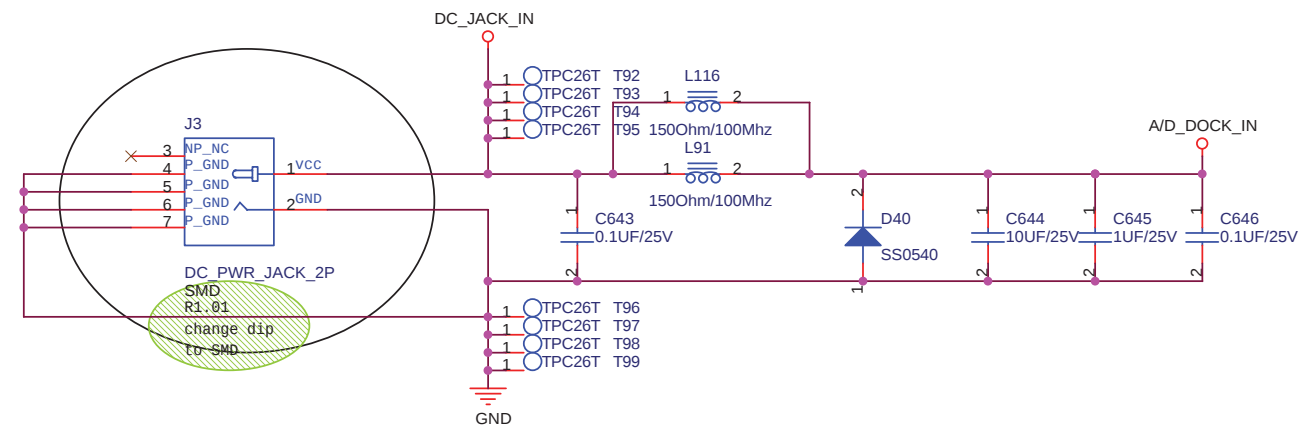
For BATTERY LED



For POWER LED

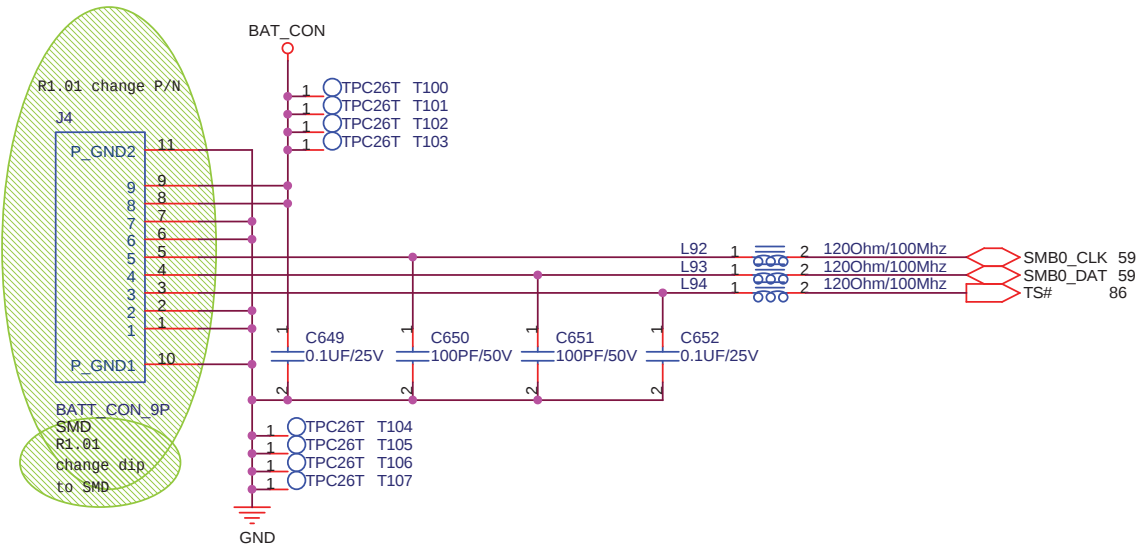


DC IN

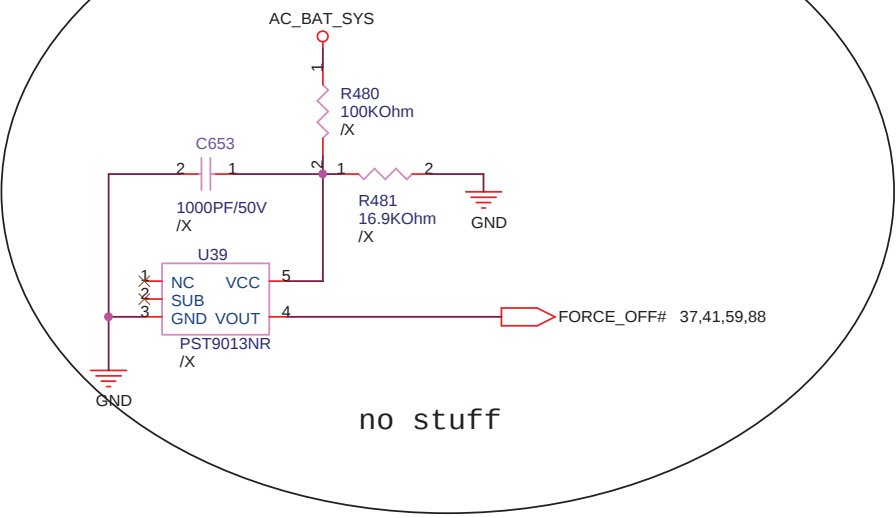


remove AC DC detect; no need

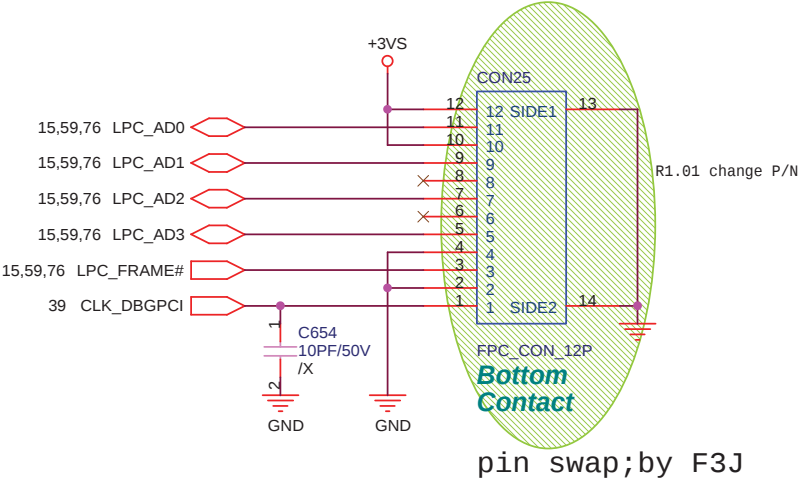
BAT IN



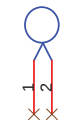
Without Battery & Pull out Adapter



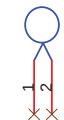
For Debug



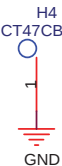
H1
2DRILL_D71N_D106N



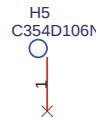
H2
2DRILL_D71N_D106N



H3
CT217b47d47p217
136N7510M270



H4
CT47CB79D47_NS



H5
C354D106N



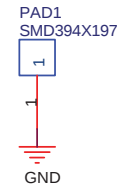
H6
C354D106N



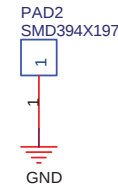
H7
C354D106N



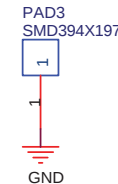
H8
C354D106N



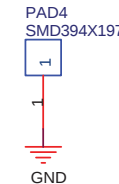
PAD1
SMD394X197



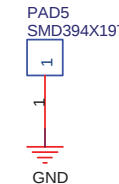
PAD2
SMD394X197



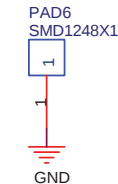
PAD3
SMD394X197



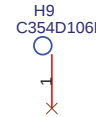
PAD4
SMD394X197



PAD5
SMD394X197



PAD6
SMD1248X197_PT



H9
C354D106N



H10
C354D106N



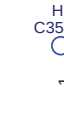
H11
C354D106N



H12
C354D106N



H13
C354D106N



H14
C354D106N



H15
C354D106N



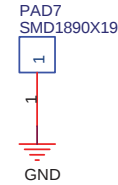
H16
C354D106N



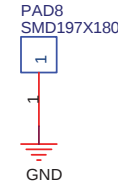
H17
C354D106N



H18
C354D106N



PAD7
SMD1890X197_PT



PAD8
SMD197X1803



H19
C354D106N



H20
C354D106N



H21
C354D106N



H22
C354D106N



H23
C354D106N



H24
C354D106N



H25
C354D106N



H26
C354D106N



H27
C354D106N

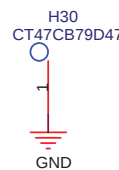


H28
C354D106N

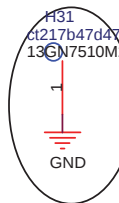
FOR SCREW HOLE



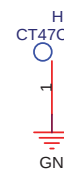
H29
CT217b47d47p217
136N7510M270



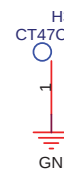
H30
CT47CB79D47_NS



H31
CT217b47d47p217
136N7510M270



H32
CT47CB79D47_NS

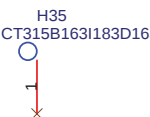


H34
CT47CB79D47_NS

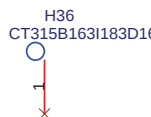


H33
CT217b47d47p217
136N7510M270

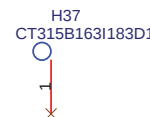
FOR SCREW HOLE



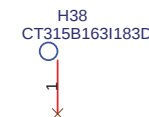
H35
CT315B163I183D163



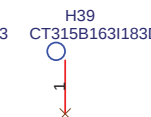
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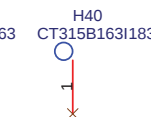
H37
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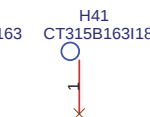
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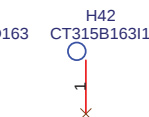
H39
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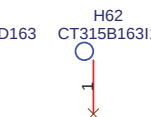
H40
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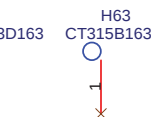
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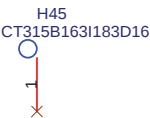
H42
CT315B163I183D163



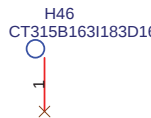
H62
CT315B163I183D163



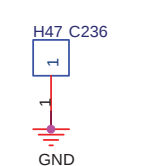
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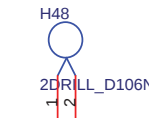
H45
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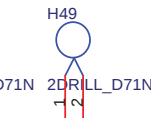
H46
CT315B163I183D163



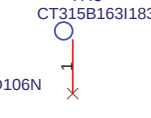
H47
C236



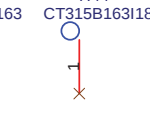
H48
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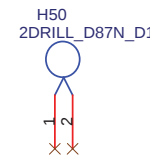
H49
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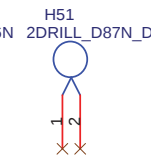
H43
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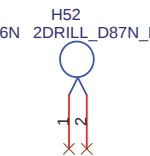
H44
CT315B163I183D163



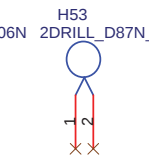
H50
2DRILL_D87N_D106N



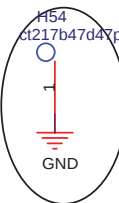
H51
2DRILL_D87N_D106N



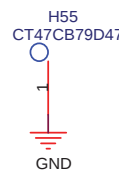
H52
2DRILL_D87N_D106N



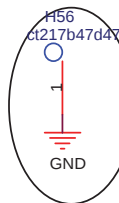
H53
2DRILL_D87N_D106N



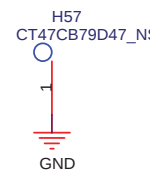
H54
CT217b47d47p217



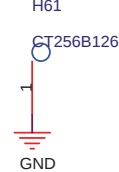
H55
CT47CB79D47_NS



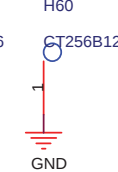
H56
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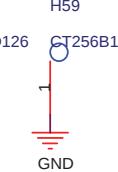
H57
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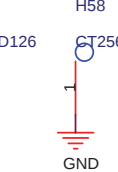
H61
CT256B126I146D126



H60
CT256B126I146D126



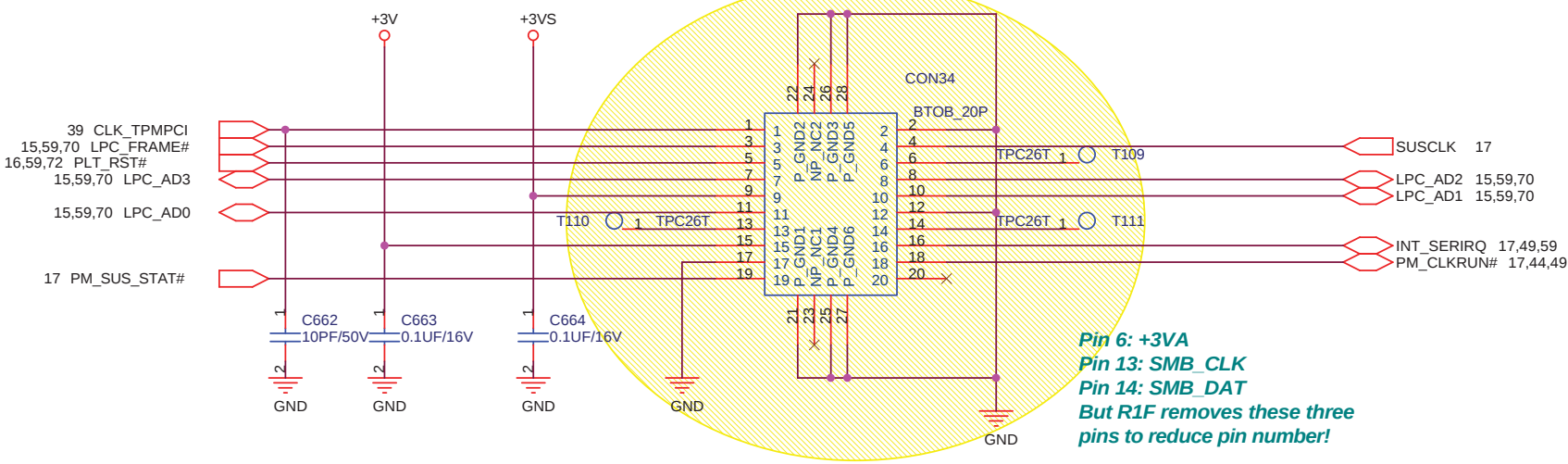
H59
CT256B126I146D126



H58
CT256B126I146D126

		Title : SREW HOLE	
ASUSTeK COMPUTER INC		Engineer: ALan Chu	
Size	Project Name	Z96J	Rev 1.0
Custom			
Date: Wednesday, January 11, 2006		Sheet	74 of 92

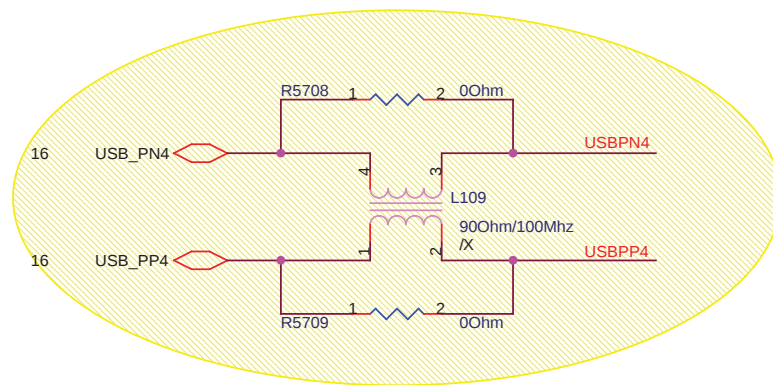
For TPM Module



Pin 6: +3VA
Pin 13: SMB_CLK
Pin 14: SMB_DAT
But R1F removes these three pins to reduce pin number!

For Bluetooth

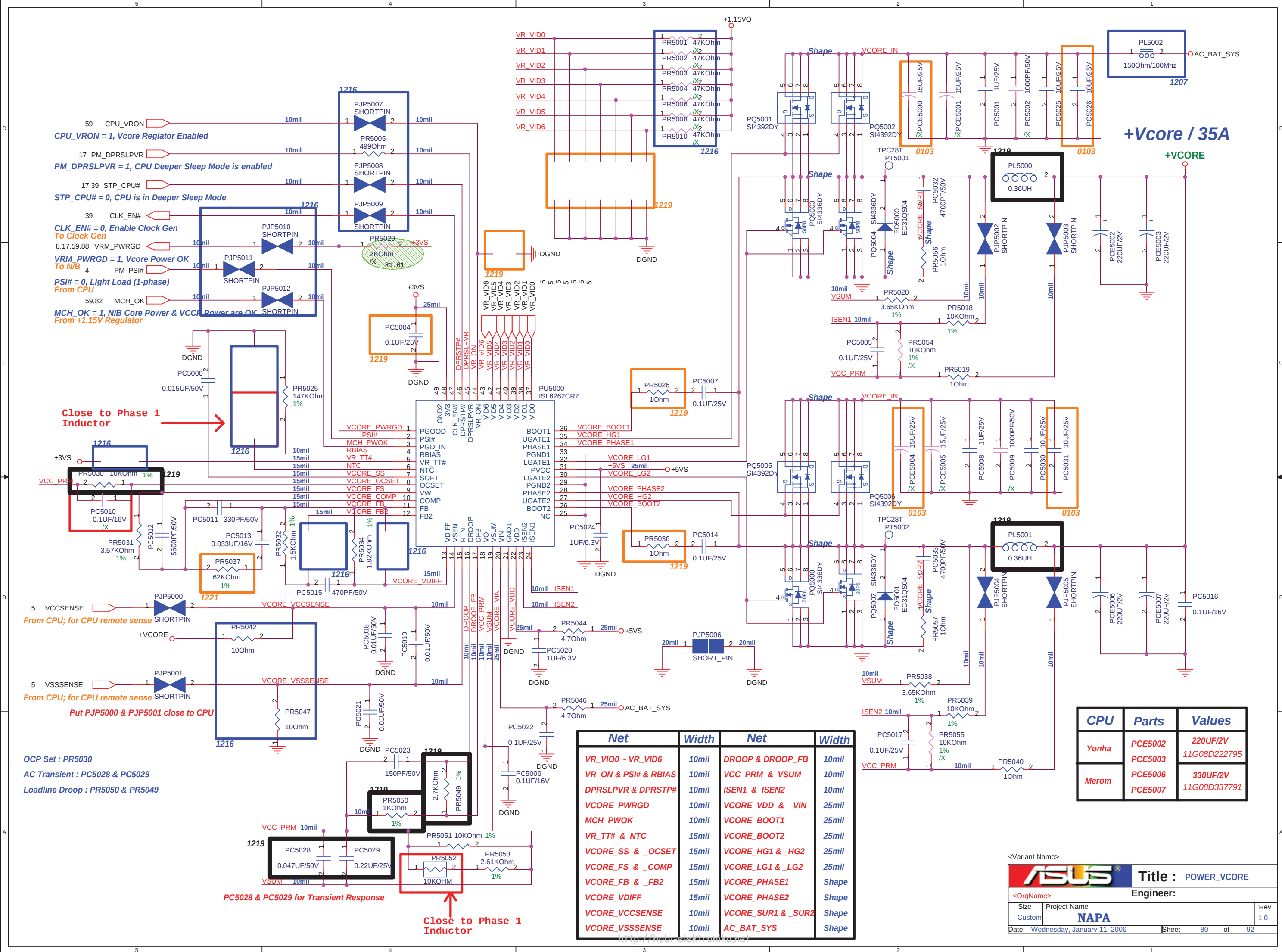
The diagram illustrates the electrical connections for a Bluetooth module. The module's pin headers are connected to a +3V supply and ground. The BT_ON/OFF# signal is connected to the module's BT_ON/OFF# pin. The BT_CHCLK and BT_CHDAT signals are connected to the module's BT_CHCLK and BT_CHDAT pins. The BT_ACTIVE signal is connected to the module's BT_ACTIVE pin. The BTLED_EN signal is connected to the module's BTLED_EN pin. The module is also connected to a USB port (USBPP4, USBPN4).

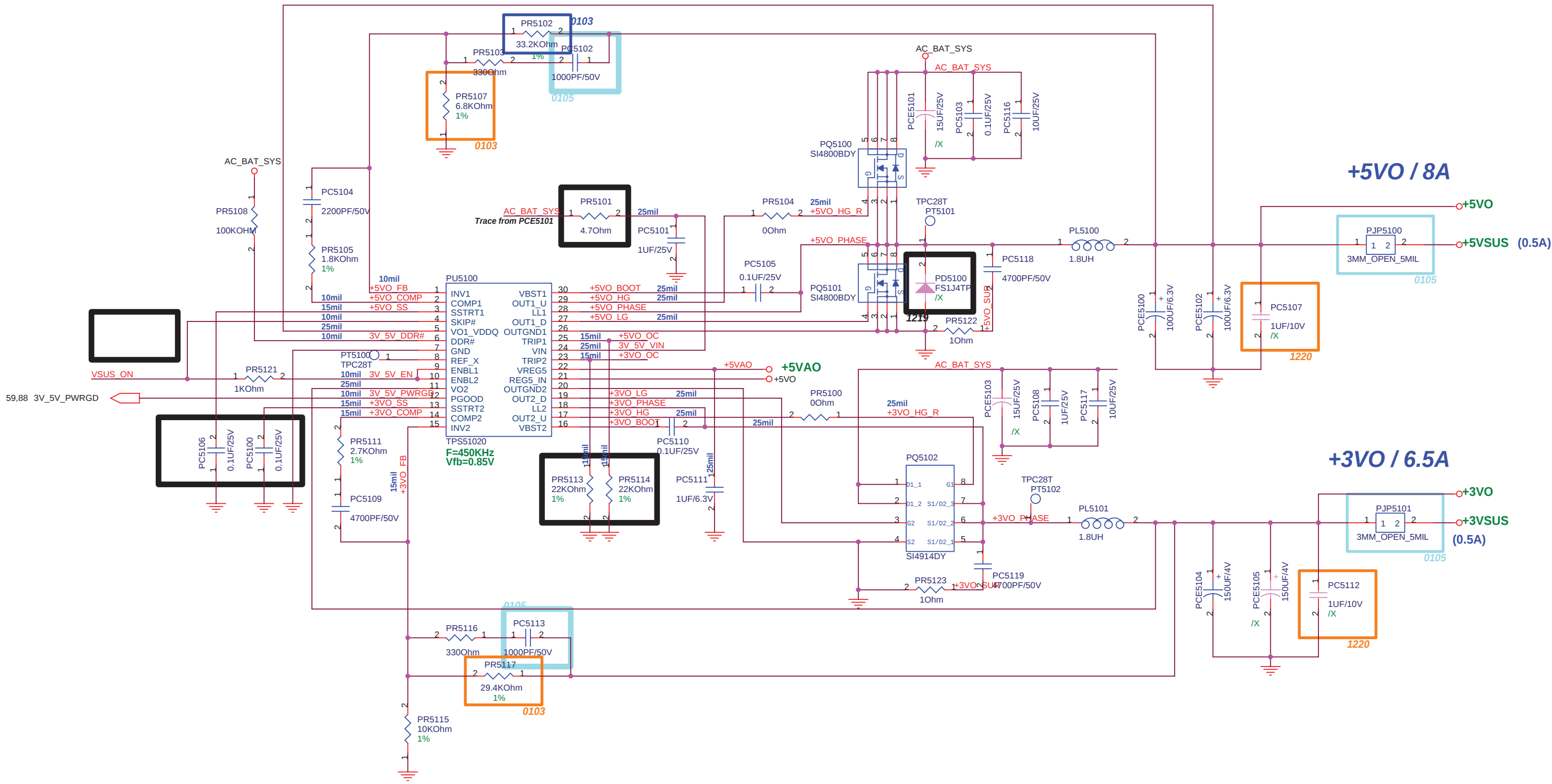


For Side SW

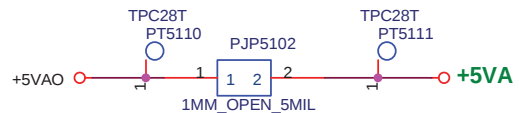
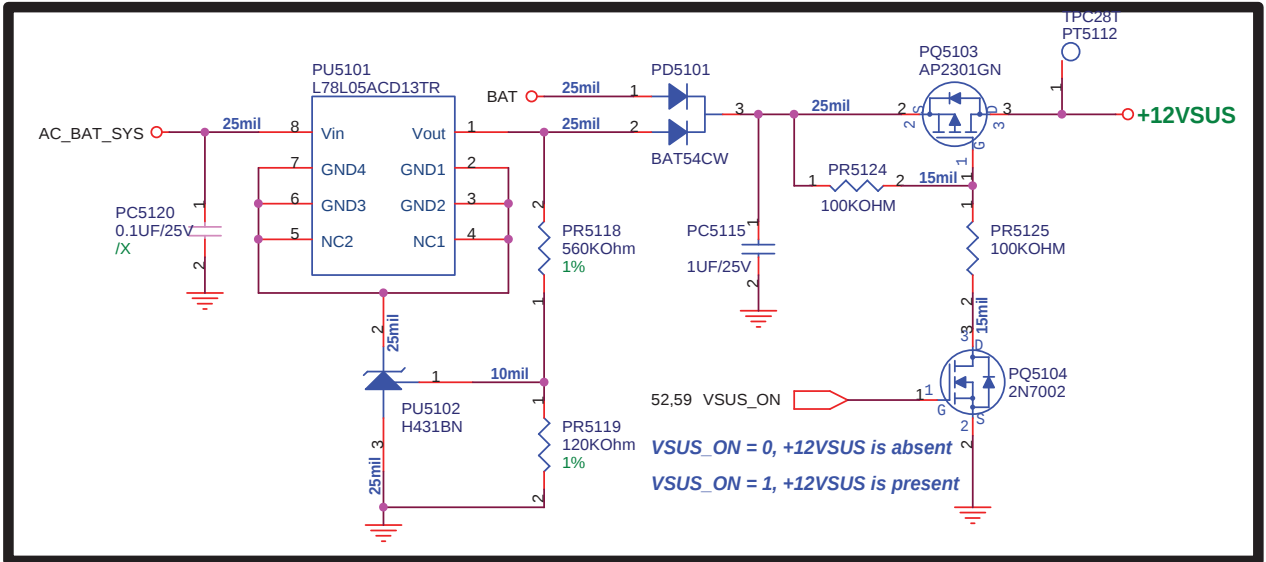
The schematic diagram for Side SW shows a circuit with the following components and connections:

- A **+3VA_EC** supply is connected to a resistor **R493** (10KOhm).
- The other end of **R493** is connected to a node labeled **47,59 RF_ON_SW#**.
- This node is also connected to a capacitor **C665** (0.1UF/16V) which is grounded.
- The node is connected to pin **1** of resistor **R494** (330Ohm).
- Pin **2** of **R494** is connected to pin **1** of a 6P switch **SW10** (SLIDE_SWITCH_6P).
- Pin **3** of **SW10** is connected to ground.
- Pin **4** of **SW10** is connected to the **+3VA_EC** supply.
- Pin **5** of **SW10** is connected to ground.
- Pin **6** of **SW10** is connected to ground.

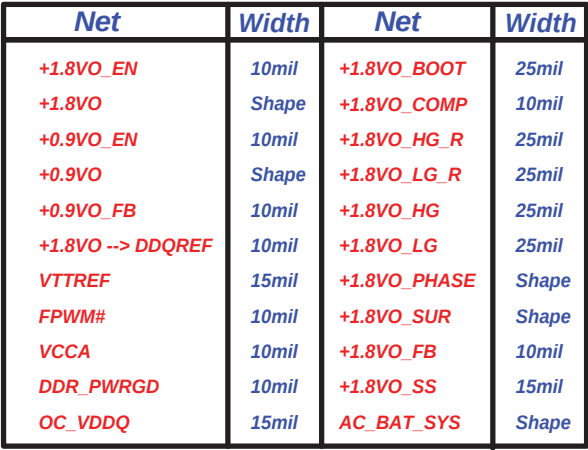




Net	Width	Net	Width
3V_5V_DDR#	10mil	AC_BAT_SYS	Shape
3V_5V_EN	10mil	+5VAO	25mil
3V_5V_PWRGD	10mil	+3VO_FB	10mil
3V_5V_VIN	25mil	+3VO_COMP	10mil
+5VO_FB	10mil	+3VO_SS	15mil
+5VO_COMP	10mil	+3VO_BOOT	25mil
+5VO_SS	15mil	+3VO_HG	25mil
+5VO_BOOT	25mil	+3VO_HG_R	25mil
+5VO_HG	25mil	+3VO_LG	25mil
+5VO_HG_R	25mil	+3VO_PHASE	Shape
+5VO_LG	25mil	+3VO_SUR	Shape
+5VO_PHASE	Shape	+3VO_OC	15mil
+5VO_SUR	Shape	+12VSUS_ADJ	10mil
+5VO_OC	15mil	+5VDRV	25mil







AC_BAT_SYS

0.1uF/25V

PC5405

PR5407 10kOhm

PR5408 10kOhm

PR5409 220Ohm

PC5406 0.1uF/25V

PT5400 TPC28T

PC5404 10uF/6.3V

PR5404 3.3kOhm 1%

PR5405 10kOhm 1%

PQ5400 MW882J3L-P

PU5401 H431BN

25mil

15mil

10mil

15mil

10mil

+3VAO

+3VAO ADJ

Imax=100mA

POWER PATH & BAT_LEARN

AC_IN Threshold 2.048Vmax A/D_DOCK_IN > 17.44V active

Adapter lin(max) = $[0.075V/Rsense(ADin)] \cdot [VCLS/VREF]$
 $Rsense(ADin) = 0.02 \text{ ohm}$
 $VCLS = 3.685V$
 $\Rightarrow \text{lin(max)} = 3.27A$
 $\Rightarrow \text{Constant Power} = 19 \cdot 3.27 = 62.13W$
 $\Rightarrow R5710 = 20K, R5715 = 137K$

Adapter lin(max) = $[0.075V/Rsense(ADin)] \cdot [VCLS/VREF]$
 $VCLS = 2.865V$
 $\Rightarrow \text{lin(max)} = 2.544A$
 $\Rightarrow \text{Constant Power} = 19 \cdot 2.44 = 48.336W$
 $\Rightarrow R5710 = 20K, R5715 = 42.2K$

Charge Current Ichg = $[0.075V/Rsense(CHG)] \cdot [VICTL/3.6V]$
 $Rsense(CHG) = 25m \text{ Ohm}$
 $VICTL = 3V \Rightarrow Ichg = 2.5A$
 $VICTL = 1.68V \Rightarrow Ichg = 1.4A$

Vbatt = Cell * { Vref + { (VCTL - 1.8V) / 9.52 } }
 $VCTL = 1.588V$
 $\Rightarrow Vbatt = 4.2V$

VICTL < 0.8V or DCIN < 7V --> Charger Disable

MODE (Pin7)	Battery
High (>2.8V)	4-Cell
Low (<0.8V)	3-Cell
High Impedance (1.6V < Vmoce < 2V)	Battery Learn

MAX8725_REF : 4.2235V
 MAX8725_LDO : 5.4V

Battery Charging Voltage :

$+V_BAT = 4 \times [4.2235 + (Vvctl - 1.8)/9.52]$

Battery Charging Current :

$I_{charge} = (0.075/PR5706) \times (Vvctl/3.6)$

Input Adaptor Max. Current Limit :

$I_{limit_current} = (0.075/PR5701) \times (Vcls/4.2235)$

Pre-Charging Mode :

Precharging current = 163.9mA

Vvctl = 0.098V

Battery Cell Selection :

BATSEL_2P# = 1, 6 Cells; Vvctl = 1.678V

$\Rightarrow I_{charge} = 2.331A$

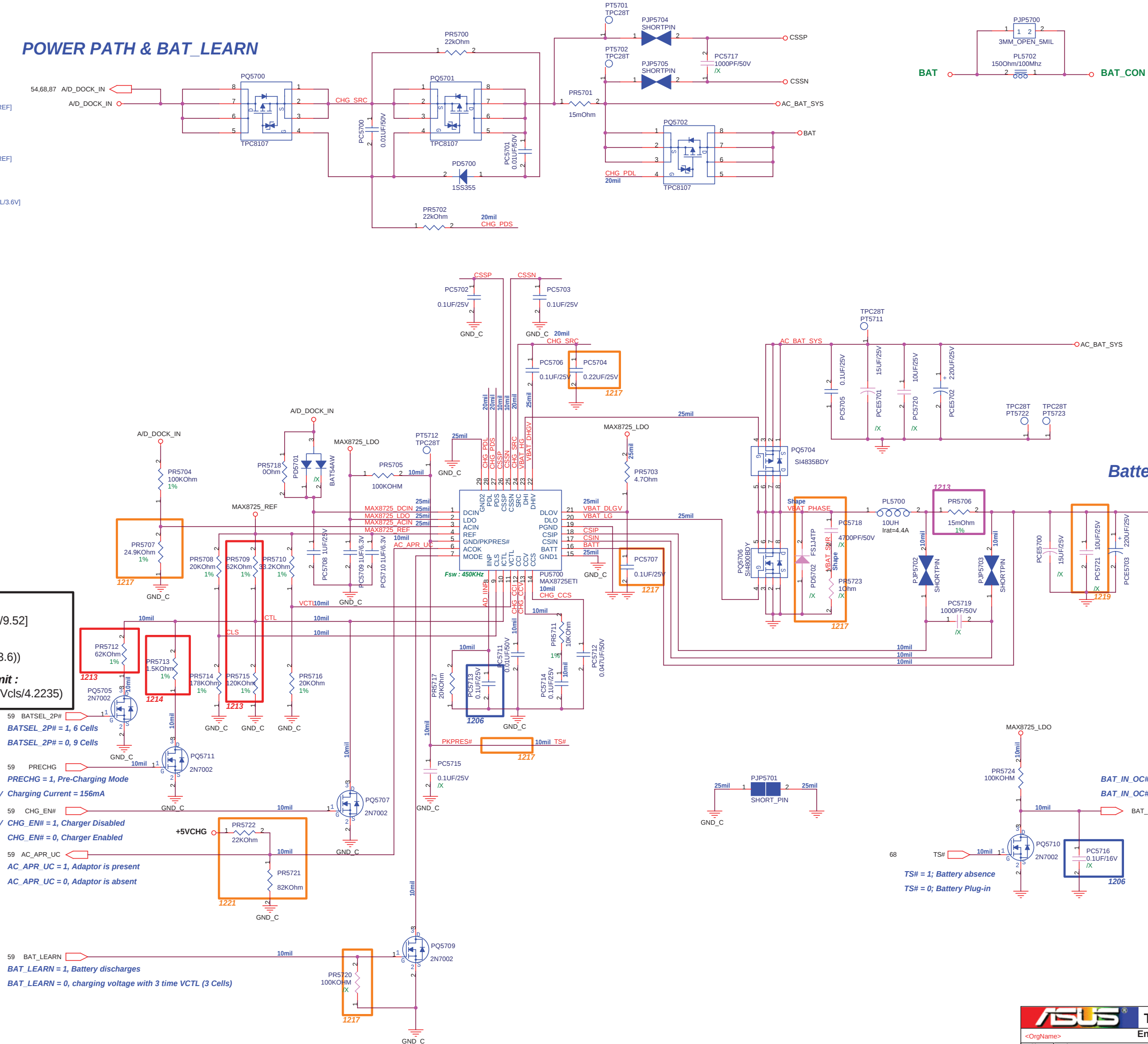
BATSEL_2P# = 0, 9 Cells; Vvctl = 2.785V

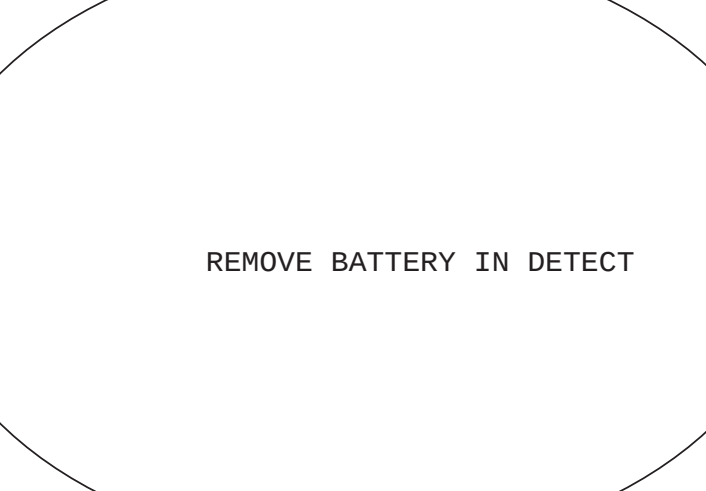
$\Rightarrow I_{charge} = 3.868A$

Adaptor Max. Current :

PR5714 = 178K; Ilimit = 4.5A; 90W

PR5714 = 47K; Ilimit = 3.5A; 65W

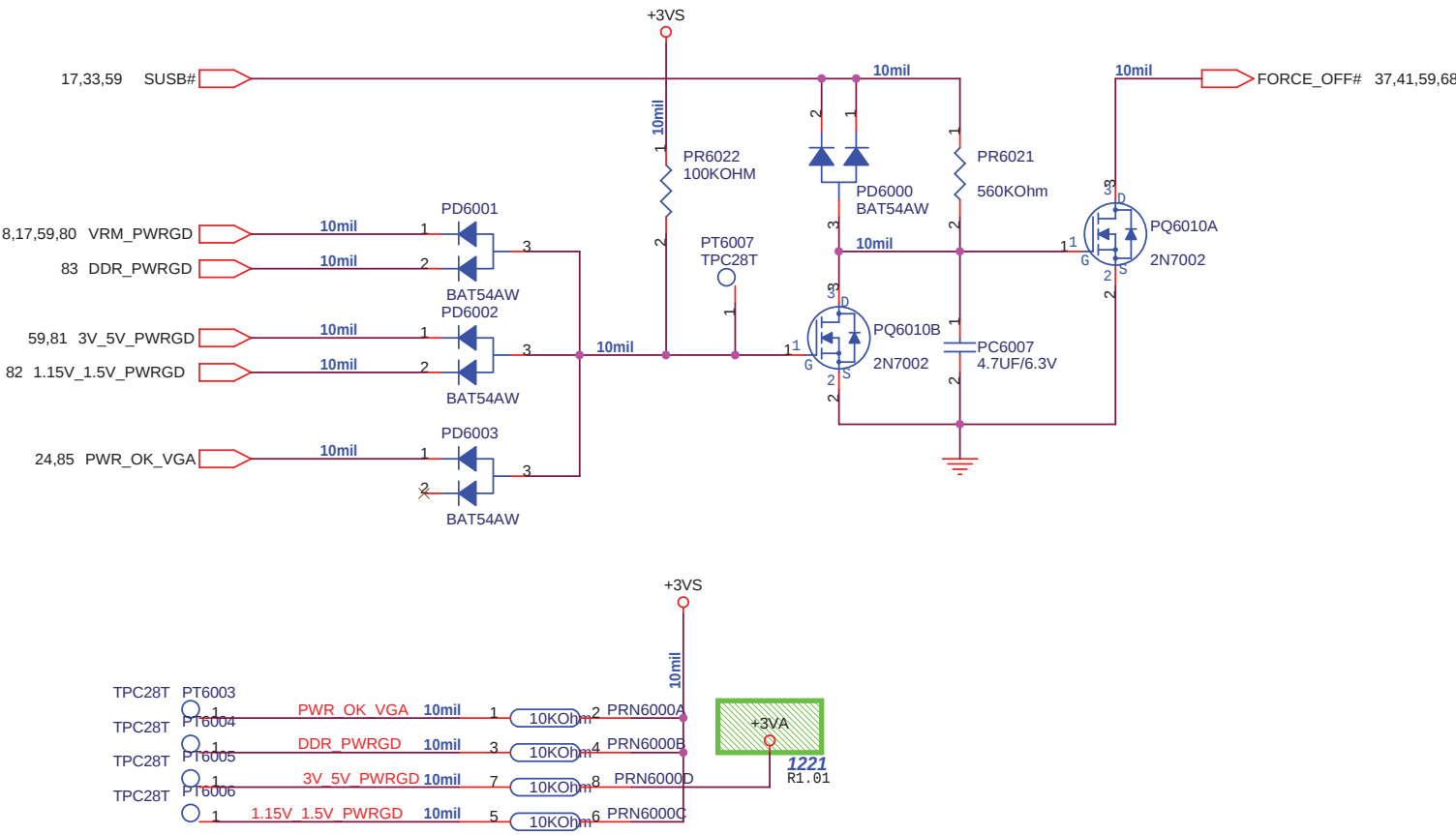




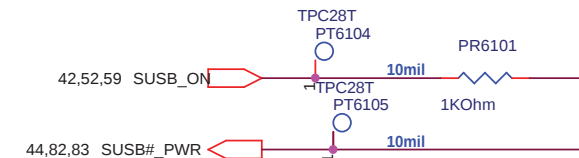
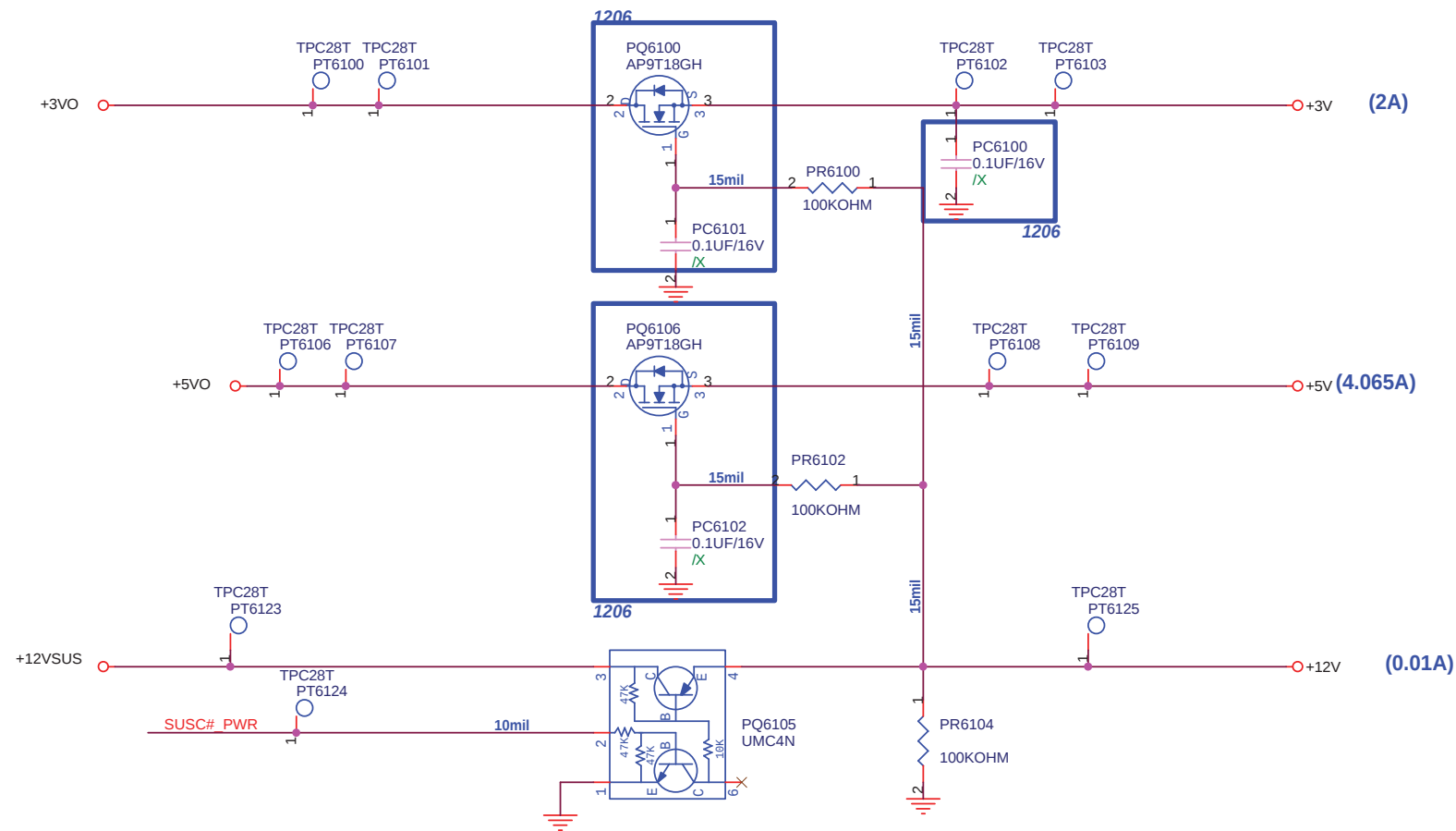
REMOVE BATTERY IN DETECT



Power Good Detector



SUSC#_PWR POWER



SUSB#_PWR POWER

